DANA

Instruction Manual

980407

SERIES 8100 AUTOMATIC COUNTERS

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ERRATA SHEET

1. Assembly Drawing 406081

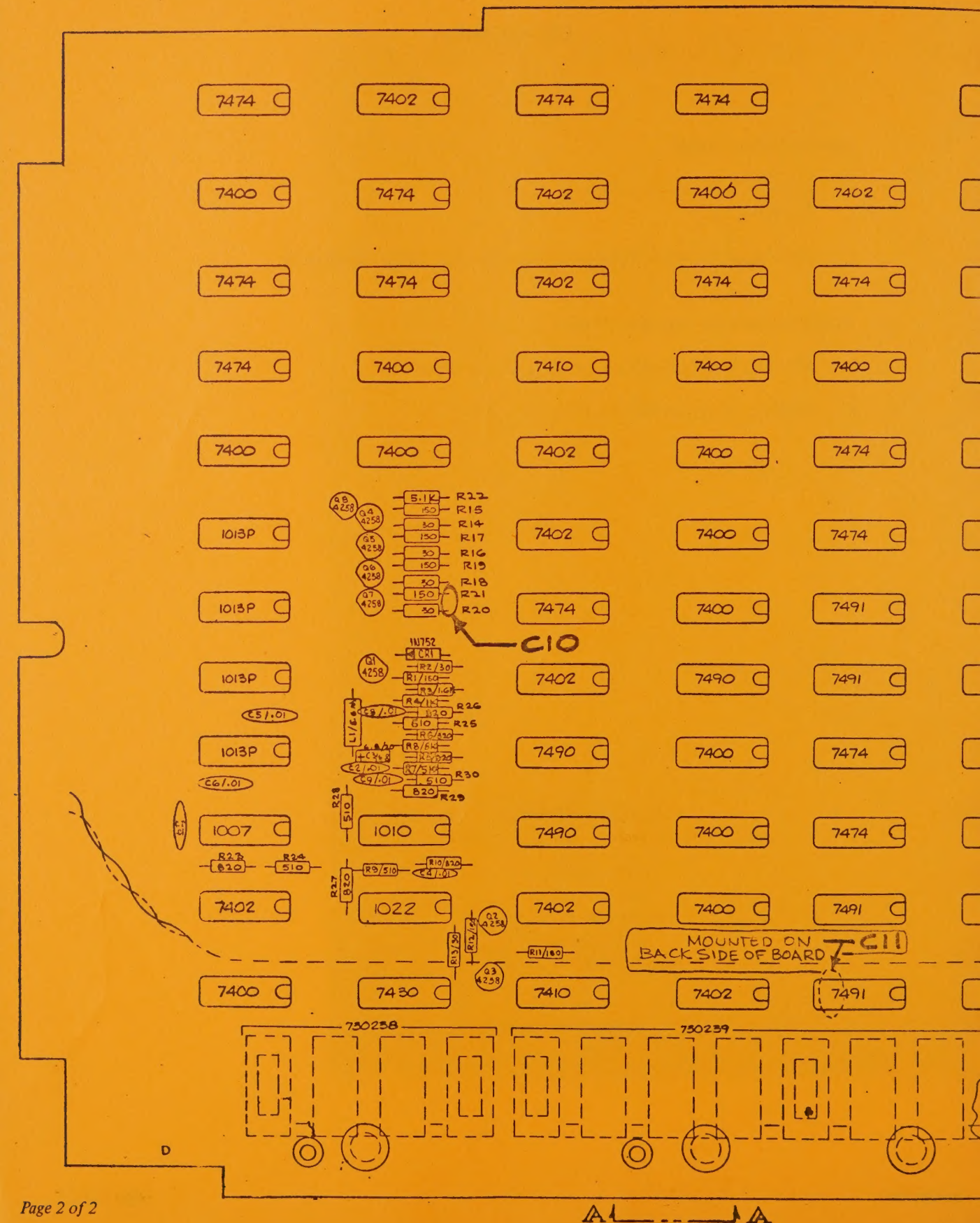
   a. R15, R17, R19, and R21 are 150;
   Should be: 110

   b. Add C10 and C11 where shown in the drawing on page 2 of this Errata Sheet.

2. Schematic, High Speed Switching, 721081

   a. Add C10, .01 μf from +5V side of R20 to Ground side of R21.

   b. Add C11, .01 μf from M3-10 to M3-5.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Q6 4258
Q7 4258
C10
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CR1
Q1 4258
R2/30
R1/100
R3/1.6K
R4/1K
R26
R25
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R24 510
R9/510
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R12/150
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R11/100
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Publication

980407

DANA

SERIES 8100

AUTOMATIC COUNTERS

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DANA®

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TELETYPE 910-595-1136
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Revised August 1974

WARRANTY

Within one year of purchase, Dana Laboratories will repair or replace your instrument, at our option, if in any way it is defective in material or workmanship. All parts and labor charges will be paid by Dana Laboratories. Just call Dana Product Service at (714) 833-1234 collect in California, for assistance. We will advise the proper shipping address for your prepaid shipment. Your instrument will be returned to you freight prepaid.

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SECTION 1

INTRODUCTION

1.1 SCOPE

This manual contains installation, operation and maintenance information for the Dana Series 8100 Automatic Counters. The measurement capability of the four basic models is shown in Table 1.1.

It is intended for use by personnel responsible for operation and/or maintenance of the equipment.

1.2 FUNCTIONAL DESCRIPTION

The Dana 8130 measures frequencies from 0.05 Hz to 500 MHz and time intervals from 0.1 microsecond to 10 seconds.

Constant 8 digit resolution is provided in one second, regardless of the input frequency. Low frequencies can be measured directly, thus eliminating the necessity of measuring period, then calculating the reciprocal to obtain frequency. Full accuracy is achieved on the first reading, with no delays for operator decisions or adjustments.

1.3 SPECIFICATIONS

The electrical and mechanical specifications are listed in Table 1.2.

1.4 MECHANICAL DESCRIPTION

1.4.1 The Dana 8130 Automatic Counter is completely self-contained in a 3-15/32" x 16-3/4" x 14" (8.9 cm x 42.4 cm x 35.6 cm) enclosure. The interior of the instrument is shown in Figure 5-1, top view, and Figure 5-2, bottom view. All circuits are mounted on printed circuit boards. The printed circuit board assemblies are the switching board, readout board, 50 MHz preamp board and 500 MHz preamp board. The power supply is mounted to the rear panel assembly.

1.4.2 All operating controls are mounted on the front panel of the counter. The BNC connectors on the front panel receive the input signal. On the rear panel are the power connector, and BNC connectors for reference input, 10 MHz reference output, and time interval trigger markers. The digital output connector is on the rear panel of models with the digital output option number 500.

Table 1.1

Dana Series 8100 Automatic Counter Selection Guide and Part List			
Model No.	Frequency to 50 MHz	Time Interval	Frequency to 500 MHz
Model 8100			
Model 8110			
Model 8120			
Model 8130			

Table 1.2 - Specifications

FREQUENCY TO 50 MHz

Range	DC Coupled .05 Hz to 50 MHz AC Coupled 5 Hz to 50 MHz
Measurement Period	1 millisecond to 10 seconds, in decade steps
Accuracy	
fx ≤ 250 kHz	$\left[\frac{\pm 1 \times 10^{-7} \pm \text{Trigger Error}\ ① \pm \text{Ref. Error}}{\text{Measurement Time}}\right]$ of reading
fx > 250 kHz	$\left[\frac{\pm 2 \times 10^{-7} \pm \text{Trigger Error} \pm \text{Ref. Error}}{\text{Measurement Time}}\right]$ of reading
Readout	Automatic ranging with units and decimal point displayed.
Input	Input "A"

TIME INTERVAL*

Range	0.1 usec to 10 seconds
Frequency Counted	10 MHz
Readout	usec
Accuracy	±.1 usec ± Reference Error ± Trigger Error ②
Inputs	Inputs "A" and "B", Separate or Common

INPUT CHARACTERISTICS

INPUT "A" OR "B"

Sensitivity (10 mV greater in counters with remote programming capability)	10 mV RMS Sine Wave 30 mV P-P Pulse, 10 nanosecond minimum Pulse Width
Impedance	1 Megohm, Shunted by 25 PF
Maximum Input	500 Volts D.C. or Peak A.C.
Trigger Level	Continuously Adjustable to ± 300% of Range
Range	.1V, 1V, 10V, 100V
Slope	+ or −
Coupling	AC or DC
Marker Outputs	Rear Panel BNC, -12V Pulse, 1 usec Wide
Preset	Selects 0 Trigger Level, 1V Range, + Slope, AC Coupling

FREQUENCY TO 500 MHz**

Range	10 MHz to 500 MHz
Measurement Period	1 millisecond to 10 seconds in decade steps
Accuracy	$\left[\frac{\pm 2 \times 10^{-7} \pm \text{Reference Error} \pm \text{Trigger Error}\ ①}{\text{Measurement Time}}\right]$ of reading
Readout	MHz
Sensitivity	1 mV RMS Sine Wave
Impedance	50 Ohms
Maximum Input	1V RMS
Automatic Gain Control	Accommodates signals up to 60 dB above threshold
"In Range" Indicator	Lights If Measurable Signal is Present
Input	Input "C"

REFERENCE OSCILLATOR

Aging Rate	$\pm 1 \times 10^{-7}$ per month
Temperature Stability	$\pm 1 \times 10^{-7}$, 20°C to 30°C; $\pm 5 \times 10^{-7}$, 0°C to 50°C
±10% Line Voltage Stability	$\pm 5 \times 10^{-8}$
Frequency Retrace	$\pm 1 \times 10^{-7}$, 30 seconds
External Reference	1 MHz, 2.5 MHz, 5 MHz, 10 MHz, 1 Volt RMS into 1 Kilohm. Automatically locks to external reference if present.
Reference Output	10 MHz Square Wave, Buffered, TTL Compatible

GENERAL

Display	8-Digits, Long Life Digital Display Tubes
Connectors	BNC
Operating Temperature	0 to 50°C
Line Power	115 Volts ± 10%, 50 Hz-60 Hz, 55 Watts Maximum
Weight	Net 15 Lb. (7 KG) Shipping 20 Lb. (9 KG)
Dimensions (H x W x D)	3-15/32" x 16-3/4" x 14" (8.9 cm x 42.5 cm x 35.6 cm)

① Trigger Error $< \frac{.3}{(S/N)\,(fx)}$ where S/N equals signal to noise ratio and fx equals input frequency

② Trigger Error < 0.0025 μsec

*8110 and 8130 only

**8120 and 8130 only

010	Rear Inputs
003	Rack Mount Adaptors
004	Add 9th Digital Display Tube (Increases Time Interval Range to 100 Seconds)

Description

Temperature Controlled Reference Oscillators					
Option No.	Aging Rate After Warmup		Warm Up*	Temperature Stability	± 10% Line Voltage Stability
	Per 24 Hours	Per Month	Hours	Per °C	
100	$3x10^{-9}$	$1x10^{-7}$	24	$1x10^{-9}$	$5x10^{-9}$
200	$1x10^{-9}$	$3x10^{-8}$	72	$1x10^{-10}$	$2x10^{-9}$
300	$5x10^{-10}$	$1.5x10^{-8}$	96	$1x10^{-10}$	$2x10^{-9}$
*after 24 hours off					

NOTES:
Dimensions in inches and (centimeters)

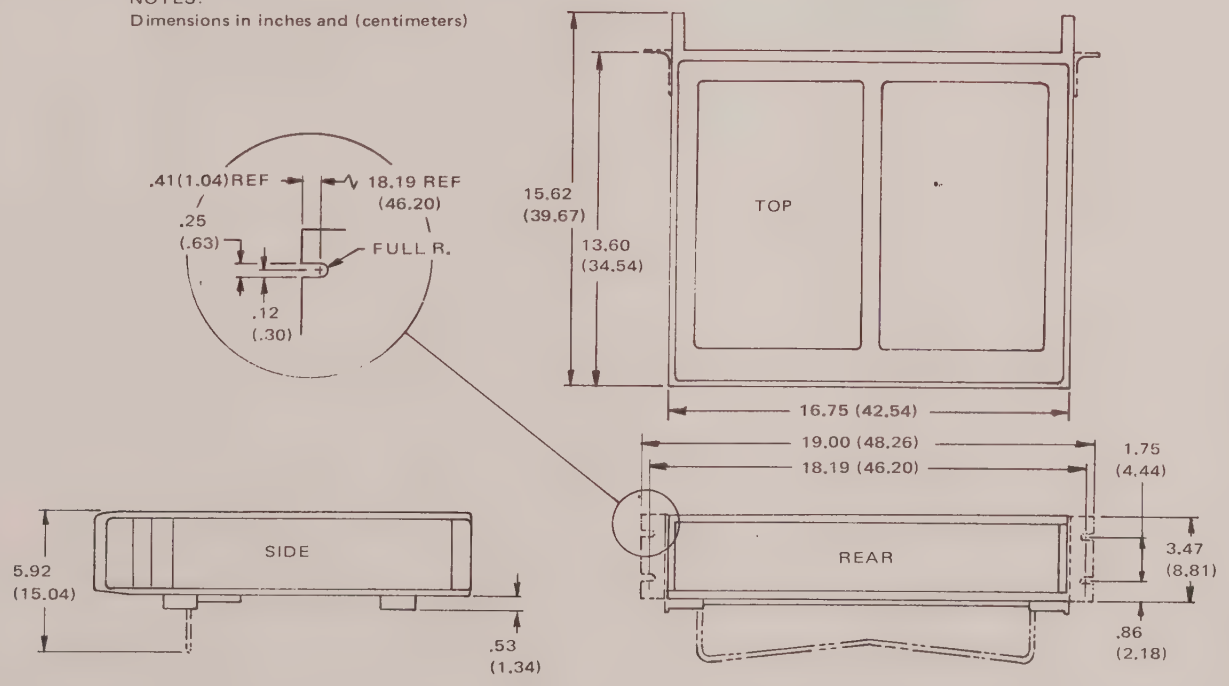


Table 1.2 - Specifications Continued

SYSTEM INTERFACE (Models 8104, 8114, 8124, 8134)

PROGRAM INPUTS	
Binary Coded Commands	Function, measurement time, input voltage range, trigger level
Single Line Commands	AC/DC, +/– slope, separate/common, hold/auto, reset
Logic Levels	Positive true, inputs are standard TTL gates
Trigger Level	
Analog	Supply ±10 VDC into 10 kilohms to set desired level; accuracy is ±5% of range ±1% of range/°C.
Digital	4 bit code, 15 steps, 20% of range per step ±140% of range, maximum; accuracy is ±5% of range ±1% of range/°C.
ELECTRICAL OUTPUTS	
Binary Coded Data	1-2-4-8 code, each data digit, plus one digit for range
Single Line Signals	Print, gate, hold/auto
Logic Levels	Positive true, from standard TTL integrated circuits

SPECIAL NOTE

The shipping carton and its internal support structure have been scientifically designed for maximum protection of the instrument. Dana recommends saving the carton and contents for use in future reshipping of the instrument. Alternate packing methods, such as plastic foam blocks and loose packing material, may prove to be insufficient for maximum protection and result in damage during shipment.

If reshipping is required and the original carton is not available, special packing instructions can be obtained from Dana Labs' Product Service Department.

SECTION 2

INSTALLATION

2.1 UNPACKING AND INSPECTION

2.1.1 The counter is bagged in a polyethylene dust cover. Four Ethafoam corner posts are pressed onto the corners. This assembly is fitted into a larger heavy duty fiberboard container which is securely taped. This form of packaging provides the instrument with a high degree of protection from normal shipping hazards. Before unpacking, examine the container for any signs of external damage. Remove the counter from the container and carefully check for any signs of damage; i.e., broken switches or knobs, scratches or dents. If damage to either the shipping container or the counter is found, notify the carrier and Dana immediately.

2.1.2 The shipping carton and its internal support structure have been scientifically designed for maximum protection of the instrument. Dana recommends saving the carton and contents for use in future reshipping of the instrument. Alternate packing methods, such as plastic foam blocks and loose packing material, may prove to be insufficient for maximum protection and result in damage during shipment. If reshipping is required and the original carton is not available, special packing instructions can be obtained from Dana Labs' Product Service Department.

2.1.3 The counter, as shipped, is designed for bench top operation. A standup bracket is provided under the case to aid in reading the visual display and operating the instrument. To adapt the counter for rack mounting, optional flanges (option 003) may be added at any time. The flanges are fitted into the grooves provided on the sides of the counter and the two locking devices on each flange are turned ¼ turn to secure the flanges.

2.2 POWER CONNECTION

An eight-foot, three-wire, power cable is supplied with the instrument. This cord connects to a three-pin power connector at the rear of the unit. Unless otherwise specified, the instrument is set up for 115 Volt, 60 cycle operation.

2.3 FUSE

The power fuse holder is located on the rear panel of the instrument and uses a 1 amp 3AG fuse.

SECTION 3

OPERATION

3.1 CONTROLS

This section describes the Series 8100 Counter Controls and Connectors. The functions of the front panel controls are as follows:

POWER. This switch applies the AC line power to the Counter. Standard Counters have a TCXO (Temperature Compensated Crystal Oscillator) for their reference oscillator. This oscillator is operating at rated accuracy (3×10^{-9}/day averaged for 30 days) 30 seconds after the power switch is activated. Optional oven oscillators (Options 100, 200 and 300) must have the POWER switch ON to maintain the oven temperature.

RESET. This switch resets the digital display to zero and arms the Counter for new reading. If the Counter is in HOLD, RESET must be activated in order to obtain a new reading.

HOLD. In this position, the Counter will hold the last reading taken. RESET must be activated for a new reading. If HOLD is actuated during the gate open time or during the compute and display update time, the Counter will complete this measurement cycle and HOLD the new reading.

AUTO. Counter continuously advances to new measurement after each compute and display update time. Previous reading is displayed while new reading is being made.

MEASUREMENT TIME. These switches select the nominal measurement times of 0.001, 0.01, 0.1, 1 and 10 seconds. On any given frequency measurement time the gate may remain open at least 3 more measurement times if necessary to complete the cycle in process. For time interval measurements, MEASUREMENT TIME becomes repetition rate. For example, with 1 second actuated, the Counter will measure the time interval and display it, then wait 1 second before taking a new time interval measurement.

REMOTE. Only used with programmable counters for REMOTE control.

FREQ A. Selects Input A for frequency measurement from 0.05 Hz to 50 MHz.

T.I.* For time interval measurements 0.1 microsecond to 10 seconds with one signal connected to Input A or with two input signals—one connected to Input A (Start trigger pulse) and one connected to Input B (Stop trigger pulse).

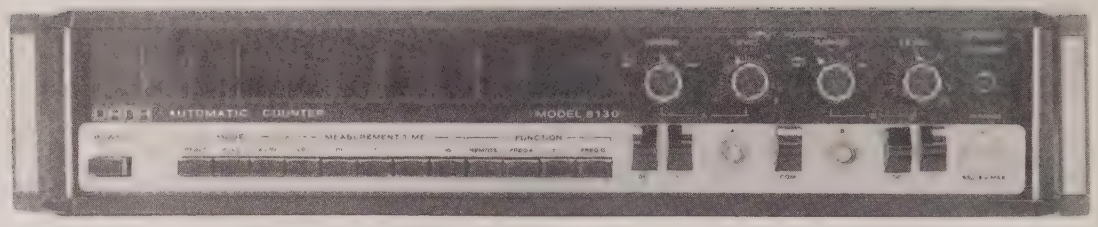
FREQ C.** Selects Input C for 10 MHz to 500 MHz frequency measurement.

RANGE. Input attenuator for Input A or Input B. In "PRESET", 1 Volt range, 0 Voltage level, AC coupling and + slope are automatically selected. For signals smaller than 100 mV or larger than 3 Volts, select the appropriate range to get noise-free triggering.

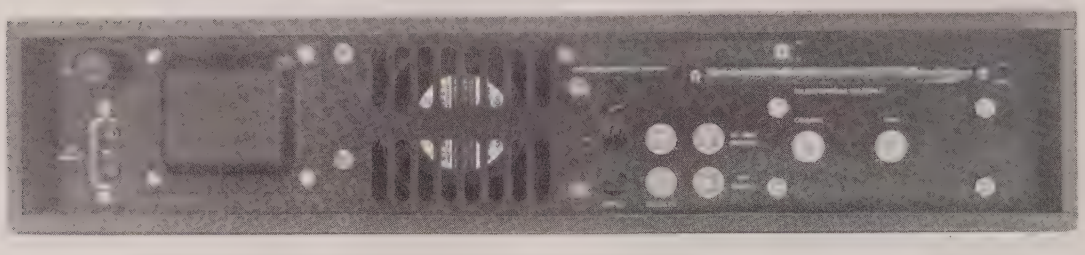
Range	Attenuation	Sensitivity (RMS)	Use For
.1	X1	10mV	10mV to 300mV
1	X10	100mV	100mV to 3V
10	X100	1V	1V to 30V
100	X1000	10V	10V to 300V

LEVEL. This control adjusts the trigger level to ± 300% of RANGE position for both Input A and Input B.

*8110 and 8130 only
**8120 and 8130 only



Front Panel



Rear Panel

AC/DC. Selects AC or DC coupling for either Input A or Input B.

+/—. Positions trigger point on positive or negative slope of signal to Input A or Input B.

SEP/COM.* This switch is only used for time interval measurements. For time interval measurements on a single waveform, switch should be in COM position and the signal applied to Input A. For time interval measurements on separate waveforms, switch should be in SEP position.

3.2 FRONT PANEL CONNECTORS

INPUT A. BNC connector for frequency measurements, 0.05 Hz to 50 MHz, or single line time interval measurements, 0.1 microsecond to 10 second.

INPUT B.* BNC connector for time interval measurements between two points on separate waveforms (INPUT B is the "stop" trigger pulse, INPUT A is the "start" trigger pulse).

INPUT C.** BNC connector for RF measurements 10 MHz to 500 MHz. Red light is energized if signal voltage is in range—minimum dynamic range is 60 dB.

3.3 REAR PANEL CONNECTORS

10 MHz OUTPUT. BNC connector for internal reference oscillator output. The output signal is a buffered, 10 MHz square wave with TTL logic levels. The output can be connected to Input A for a self test. Reading should be 10.000000 MHz.

REF INPUT. BNC connector for operating the Counter with an external 1 MHz, 2.5 MHz, 5 MHz or 10 MHz standard. Input 1 volt into 1 kilohm. If an external signal is connected but is not present, the Counter will automatically operate from internal reference oscillator.

A & B MARKERS. BNC connectors for setting trigger level accurately by intensifying an oscilloscope trace using the Z-axis input. The markers are -12 Volt, 1 microsecond wide pulses.

AC LINE. Connection for 3-wire AC power cord.

*8110 and 8130 only
**8120 and 8130 only

3.4 FREQUENCY MEASUREMENTS 0.05 Hz TO 50 MHz (INPUT A)

For measurement of sine waves, above 5 Hz between 100 mV and 3V rms put the RANGE control in PRESET for automatic signal conditioning. However, for lower frequencies, pulses or large or small signals, stable and calibrated triggering adjustments are available for optimum signal conditioning.

DC coupling should be used for sine waves below 5 Hz or for pulses.

The LEVEL control adjusts the trigger set point between -300% and +300% of the RANGE control setting. The RANGE control should be set properly so that triggering on noise is minimized. See RANGE section of 3.1. In the + slope position, triggering will occur when the signal rises to the selected trigger voltage level; conversely, in the — slope position, triggering will occur when the signal falls to the selected trigger voltage level.

Example:	RANGE	.1
	LEVEL	2.5
	AC/DC	AC
	+/—	+

With the above settings on the input controls, triggering will occur when the input signal rises to +.25 volts. By the use of the -12 volt MARKER pulse as an intensifier on a dual trace oscilloscope (Z-Axis), it is possible to precisely set the trigger set point.

Select FREQ A, the appropriate MEASUREMENT TIME, and mode of operation—either HOLD (RESET must be activated for a new reading) or AUTO (automatic recycling after each measurement). On any given MEASUREMENT TIME, the gate remains open to complete the last cycle being processed (an exact number of cycles is always counted). The gate may remain open a maximum of 4 measurement times to process this last cycle. If signal is lost, the display will reset to zero. Therefore, the lowest frequency measured is a frequency whose period is 4 times the selected MEASUREMENT TIME of 1 second selected, the lowest frequency which can be measured on this MEASUREMENT TIME is 0.25 Hz.

3.5 TIME INTERVAL MEASUREMENTS*

Intervals from 100 nanoseconds to 10 seconds (100 seconds with addition of 9th digital display tube Option 004) with a resolution of 100 nanoseconds can be measured.

For time interval measurements on a single waveform, apply signal to INPUT A and put SEP/COM switch to COM. For time interval measurements on separate waveforms, connect the start signal to INPUT A and the trigger stop pulse to INPUT B and the SEP/COM switch to SEP.

Two identical input circuits provide stable and calibrated trigger level control for both independent channels. Trigger level is adjusted for both channels by the same procedure used in "Frequency Measurements 0.05 Hz to 50 MHz".

3.6 RF FREQUENCY MEASUREMENTS (INPUT C)**

The counter can measure frequencies from 10 MHz to 500 MHz automatically. When a signal is applied to INPUT C, it is prescaled by 10 and read directly on the digital display tubes. For example, a 500 MHz signal would be displayed as 500.00000 MHz for a 1 second measurement time.

An AGC loop automatically attenuates the input waveform. Loop bandwidth is 10 kHz. The AGC circuit has a minimum of 60 dB dynamic range. For example, for signals from 1 mV to 1V, the IN RANGE light will remain lit and the counter will measure the frequency accurately and automatically. The effective operating range of the AGC loop can be easily altered by using an external attenuator. With an X10 attenuator (e.g., Tektronix 011-0059-01), the effective range is 10 mV to 10V, and with an X5 attenuator, (Tektronix 011-0060-01) the range is 5 mV to 5V.

*8110 and 8130 only
**8120 and 8130 only

Because of this excellent sensitivity, it is now possible to measure amplitude modulated (AM) signals. See Figure 3-1.

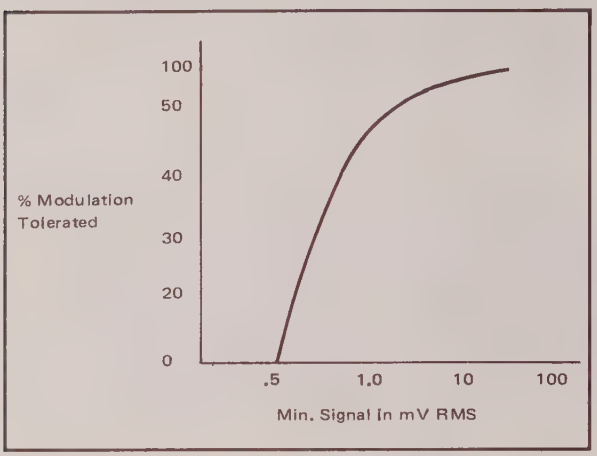


Figure 3-1

Frequency modulated (FM) signals can also be tolerated as long as the frequency components are within 10 MHz to 500 MHz. Average frequency will be displayed for a given measurement time: i.e., the carrier frequency.

3.7 ELECTRICAL OUTPUT (OPTION 500)

The Counter is available with an optional BCD 1-2-4-8 output. Standard logic levels are TTL with the "1" level from 2.4 to 4.0 volts and the "0" level from 0 to 0.4 volts. Table 3-1 describes the pin connections.

For a zero logic level, the output accessory can sink up to 10 ma. For a One logic level, the output can supply up to 200 μamps.

Table 3-2 is a truth table of the BCD output. Table 3-3 shows examples of frequency and Time Interval outputs and how they are interpreted.

3.8 REMOTE PROGRAMMING (Models 8104, 8114, 8124, 8134 only).

The above models can be remotely programmed through the PROGRAMMED INPUT connector

Table 3-1 - Electrical Output - Pin Assignments

Pin No.	Bit	Description	Pin No.	Bit	Description
1	4	Decimal Point	A		High Reference
2		Ground	B	8	Decimal Point
3	2	Decimal Point	C	1	Decimal Point
4	4	First Digit*	D	4	Second Digit
5	2	First Digit	E	2	Second Digit
6	1	First Digit	F		Unused
7	8	First Digit	H		Unused
8	8	Second Digit	J	1	Second Digit
9		Unused	K		Unused
10	2	Third Digit	L	4	Third Digit
11	2	Fourth Digit	M	4	Fourth Digit
12	8	Third Digit	N	1	Third Digit
13	8	Fourth Digit	P	1	Fourth Digit
14	2	Fifth Digit	R	4	Fifth Digit
15	2	Sixth Digit	S	4	Sixth Digit
16	8	Fifth Digit	T	1	Fifth Digit
17	8	Sixth Digit	U	1	Sixth Digit
18	2	Seventh Digit	V	4	Seventh Digit
19	2	Eighth Digit	W	4	Eighth Digit
20	8	Seventh Digit	X	1	Seventh Digit
21	8	Eighth Digit	Y	1	Eighth Digit
22	2	Ninth Digit	Z	4	Ninth Digit
23		Remote	AA		Gate
24	8	Ninth Digit	BB	1	Ninth Digit
25		Auto	CC		Print

* First digit is least significant digit; digits are numbered right to left.

Mating Connector: Dual 25, Cinch 251-25-30-160, supplied with unit.

(J13) on the rear panel. Command logic levels are:

One = 2.4 to 5.0 volts
Zero = 0 to 0.4 volts

The TTL input lines are equipped with 2-kilohm pullup resistors so that contact closures to ground can be used to generate a command. For a Zero logic level, the source must be capable of sinking 8 ma, minimum. A supply of 160 μamps, minimum, is required for a logic One level.

Pin assignments of the PROGRAMMED INPUT connector are listed in Table 3-4. A truth table of the logic on the input lines is shown in Table 3-5. Table 3-6 is an example of a typical program. Timing considerations are shown in Table 3-7.

Table 3-2 - Electrical Output Truth Table

DIGIT READOUT	BCD 8 4 2 1 POSITIVE LOGIC CODE ON LINES INDICATED BELOW
	8 4 2 1
9 — MSD in 9-digit model	24 Z 22 BB
8 — MSD in 8-digit model	21 W 19 Y
7	20 V 18 X
6	17 S 15 U
5	16 R 14 T
4	13 M 11 P
3	12 L 10 N
2	8 D E J
1 — Least significant digit	7 4 5 6
DECIMAL POINT	
Frequency — floating point	
— Assume decimal point one place right of MSD	
— Exponent	B 1 3 C
— Answer in Hz	
Time interval — fixed point	
— Assume fixed decimal point one place left of LSD	
— Answer in usec.	
MODE INDICATORS	
Gate	
Logic "1" while counting	AA
Print	
Logic "1" for print **	CC
Auto	
Logic "1" while in Auto	25
Remote	
Logic "1" while in Remote	23
	Utility Line
Ground or low reference	2
2.5 VDC or high reference	A

**Falls to "0" for at least 20 microseconds before rising to "1" state

Table 3-3 - Examples - Frequency Output Codes

Frequency reading The following pins have "1" logic levels on the output:

W, Y, 18, 14, T, L, 8, 3, C, CC (reading completed)
The frequency is 5.2030480×10^{3} Hz, or 5.2030480 KHz.

Time interval reading The following pins have "1" logic levels on the output:

L, D, J, 5 , CC (reading completed)
The time is 45.2 usec.

Table 3-4 - Programming Input - Pin Assignments

Pin No.	Description	Pin No.	Description
1	Channel B Slope	A	Channel B Trigger Level
2	Channel B Coupling	B	Channel B Trigger Level
3	Channel B Input Range	C	Channel B Trigger Level
4	Channel B Input Range	D	Channel B Trigger Level
5	Channel A Input Range	E	Channel B Trigger Level
6	Channel A Slope	F	Channel A Trigger Level
7	Unused	H	Channel A Trigger Level
8	Ground	J	Channel A Trigger Level
9	Unused	K	Channel A Trigger Level
10	Unused	L	Channel A Trigger Level
11	Unused	M	Channel A Coupling
12	Unused	N	Channel A Input Range
13	Unused	P	Reset
14	Unused	R	Auto/Hold
15	Unused	S	Measurement Time
16	Separate/Common	T	Function
17	Function	U	Measurement Time
18	Unused	V	Measurement Time
Mating Connector: Dual 18 pin, Cinch 251-18-30-160, supplied with unit.			

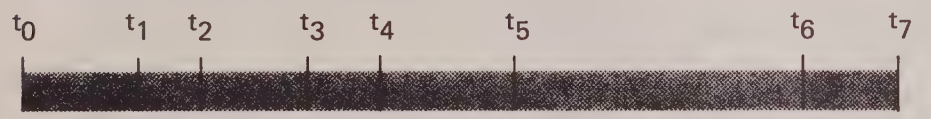
Table 3-5 - Programming Input - Truth Table

ITEM	PIN CONNECTIONS			IDENTIFICATION CODE
		Channel A	Channel B	
Mode	R			Auto 0 / Hold 1
	P			Reset 1
Measurement Time (seconds)				0.001 / 0.01 / 0.1 / 1 / 10
	U			0 1 0 1 0
	V			0 0 1 1 1
	S			0 0 0 0 1
Function				Frequency A 0 / T.I. 1 / Frequency C 0
	17			0 1 0
	T			0 0 1
Input Range (volts)				0.1 / 1 / 10 / 100
		5	4	0 1 0 1
		N	3	0 0 1 1
Trigger Level (x 20% of range)				7 6 5 4 3 2 1 0 1 2 3 4 5 6 7 8
		F	B	0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1
		H	C	0 0 1 1 0 0 1 1 0 0 1 1 0 0 1 1
		J	D	0 0 0 0 1 1 1 1 0 0 0 0 1 1 1 1
		K	E	0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1
		L	A	Analog Line — ± 10 VDC into 10K ohms gives ± 200% of range
Coupling	16			Sep 1 / Com 0
				AC 1 / DC 0
		M	2	
Slope		6	1	+ Slope 1 / Slope 0

Table 3-6 - Example - Typical Program

Item	Condition	Pin. No.	Logic Level
Mode	Hold	R	1
To Command Single Reading at t_0	Reset	P	1
Measurement Time	1 Sec	U	1
		V	1
		S	0
Function	Freq. A	17	0
		T	0
Input Range	1 volt	5	1
		N	0
Trigger Level, digital	−.4 volts	F	1
		H	0
		J	1
		K	0
Coupling	Sep.	16	1
	AC	M	1
Slope	+	6	1
Trigger Level, analog	0 volts	L	0 volts

Table 3-7 - Program Timing



t_0 Set all controls including "Reset" to appropriate logic levels.

$t_1 - t_0$ Time required for commanding system to settle within TTL voltage ranges.

$t_2 - t_1$ Time required for counter to react to various programming commands is as follows:

PROGRAM COMMAND	TIME REQUIRED
Attenuator position	
.1 V ↔ 100 V	10 ms
.1 V ↔ 10 V	1.5 ms
.1 V ↔ 1 V	.5 ms
Sep/Com	40 ms
Input coupling	
DC ↔ AC	.5 ms
DC level present	500 ms additional
Trigger slope	
+ ↔ −	.015 ms
Trigger level	
Binary code	2.5 ms max
Analog voltage	.005 ms max.
Function, range, and mode	100 ns

t_2 Remove "Reset."

$t_3 - t_2$ Time required for commanding system to settle.

$t_4 - t_3$ 100 nanoseconds for counter to react to removal of "Reset."

$t_5 - t_4$ 4 microseconds for counter to clear and arm for a new reading.

$t_6 - t_5$ Counter measurement time maximum time is 400% of selected measurement time.

$t_7 - t_6$ 200 microseconds for computation.

t_7 Print command from counter.

Should the counter remain in a hold mode, a reset must be programmed every time a new reading is required. Should the counter be in an auto mode, the counter automatically recycles.

SECTION 4 THEORY OF OPERATION

4.1 GENERAL.

4.2 This section presents the theory of operation of Series 8100 Automatic Counters. Two levels of discussion are presented. Paragraphs 4.3 through 4.42 describe overall theory of operation with reference to block diagrams. Paragraphs 4.43 through 4.238 provide a detailed description of the operation of logic and analog circuits with reference to the logic and schematic diagrams contained in Section 8 of this manual.

4.3 OVERALL BLOCK DIAGRAM (See Figure 4.1).

4.4 Functionally, the automatic counter consists of the following sections:

a. Input circuits which amplify input waveforms and provide square wave shapes for counting.

b. Counting and arithmetic logic which develops the frequency measurement or time interval measurement data.

c. Control logic which conditions the counting and arithmetic logic to perform the selected function and to operate in the selected mode.

d. Readout logic which provides storage for the measurement data developed by the counting and arithmetic logic and provides drive for the digital display.

e. Time base circuits which provide a 10 MHz time base signal derived either from an internal oscillator or from the harmonics of a 1 MHz, 2.5 MHz, 5 MHz, or 10 MHz external reference input.

f. Optional electrical output circuits which supply BCD digit data, exponent data defining the significance of the magnitude data, and status signals to external equipment.

g. Mode, function, and signal conditioning selection facilities. On models whose number ends in 0, these facilities are limited to the controls on the front of the unit. Models whose numbers end in 4 have the capability of accepting remote programming inputs when the REMOTE mode is selected on the front of the unit.

4.5 The basic input circuit of the unit is the 50 MHz trigger amplifier which accepts the signal applied to the INPUT A connector on the front of the unit. With this input circuit, the unit is capable of measuring input frequencies up to 50 MHz. With appropriate signal conditioning selections, the 50 MHz trigger amplifier can accept signal inputs over the range from 10 mV to 100 volts.

4.6 An input circuit which extends the range of the unit to the measurement of frequencies up to 500 MHz is the 500 MHz prescaler circuit which is provided on models 812X and 813X. This circuit is provided with automatic gain control which permits input signals to be anywhere within the range from 1 mV RMS to 1V RMS. The prescaler divides the input frequency by 10 in order to provide the 50 MHz maximum frequency that can be processed by the remainder of the unit.

4.7 Models 811X and 813X are equipped with a second 50 MHz trigger amplifier channel. This extends the capability of the unit to allow the performance of time interval measurements. For time interval measurements, the TRIGGER A signal from channel A defines the start of the interval while the TRIGGER B signal from channel B defines the termination of the interval. In accordance with the status of the SEP/COM selection, channel B may receive its input from a separate INPUT B connector or may receive the signal being supplied to channel A from the INPUT A connector. Thus, the interval between signals on separate lines or the interval between two signals on the same line can be measured. Further versatility is obtained by means of the +/– slope and trigger-level selections which allow the unit to trigger on either the positive or negative slope of the input and permit the triggering threshold to be adjusted over a wide range. Separate slope and trigger-level selections can be made for the two channels.

4.8 FREQUENCY MEASUREMENT.

4.9 In order to make a frequency measurement, the unit first accumulates counts of the unknown frequency and of a known time base over an interval whose nominal length is selected as the MEASUREMENT TIME. (See figures 4.2 and 4.3.) Counting is enabled when the GATE signal is true. The setting and resetting of the GATE signal is accomplished using true-going transitions of the unknown frequency signal. Thus, counting is always enabled for an integral number of periods of the unknown frequency. As a consequence, there is no uncertainty about the number of cycles of the unknown frequency that are counted.

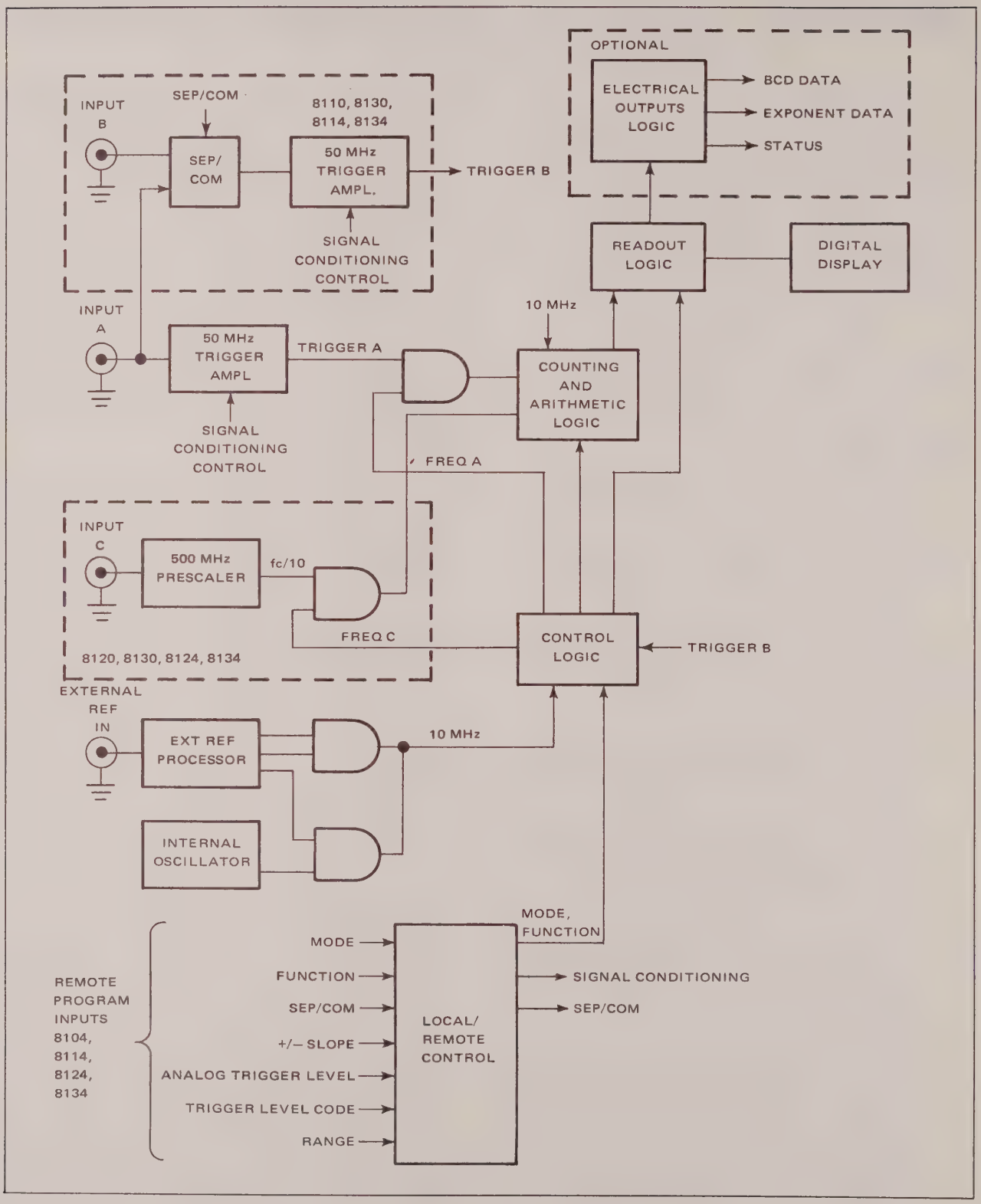


Figure 4.1 - Series 8100 Automatic Counter, Block Diagram

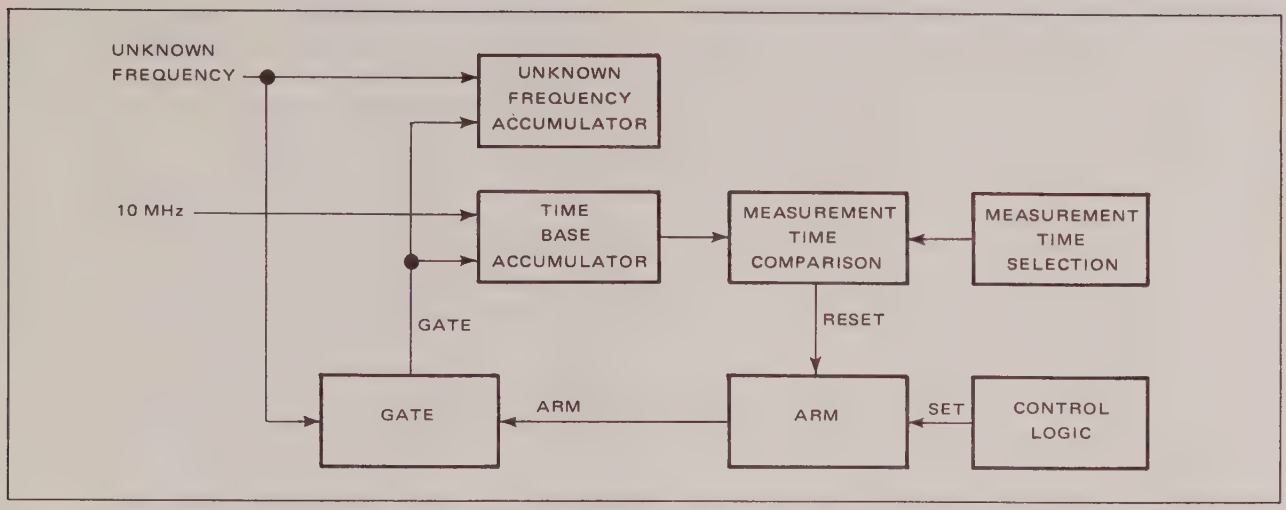


Figure 4.2 - Frequency Counting Logic, Block Diagram

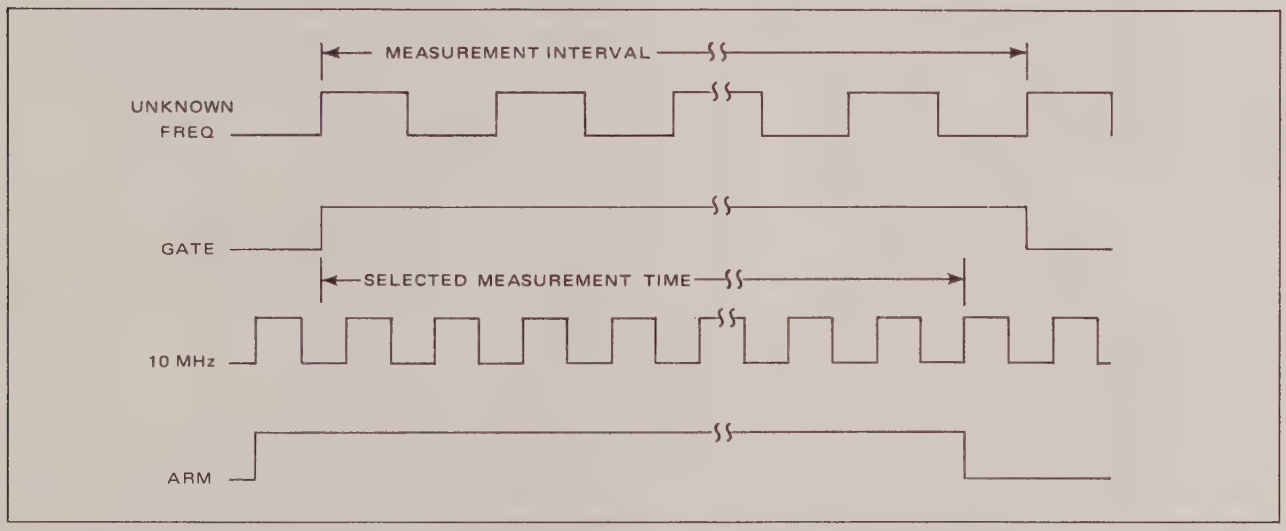


Figure 4.3 - Measurement Interval Timing

4.10 The unknown frequency is enabled to set or reset the GATE signal by the ARM signal. At the start of a measurement, the ARM signal is set by the control logic. With ARM true, GATE is set by the next true-going transition of the unknown frequency signal. With GATE true, counts of the unknown frequency and of the 10 MHz time base signal are accumulated. The time base count is continuously compared with the selected MEASUREMENT TIME data. When the accumulated time base count is equal to the selected MEASUREMENT TIME, the measurement time comparison logic resets the ARM signal. The next positive-going transition of the unknown frequency signal then resets the GATE signal and terminates counting.

4.11 While the measurement time interval lasts for an integral number of cycles of the unknown frequency, it does not necessarily last for an integral number of cycles of the 10 MHz time base, nor is this time base synchronized with the unknown frequency. Thus, there is an uncertainty of one period or 100 nanoseconds in the time base count. Assuming that the measurement interval has a nominal length of 10 seconds, this is an uncertainty of 1 part in 10^8. This uncertainty accounts for the multi-digit flicker that is observed in the least significant digit position of the counter when the unit is operated in the AUTO mode so that new measurements are continuously being completed and displayed.

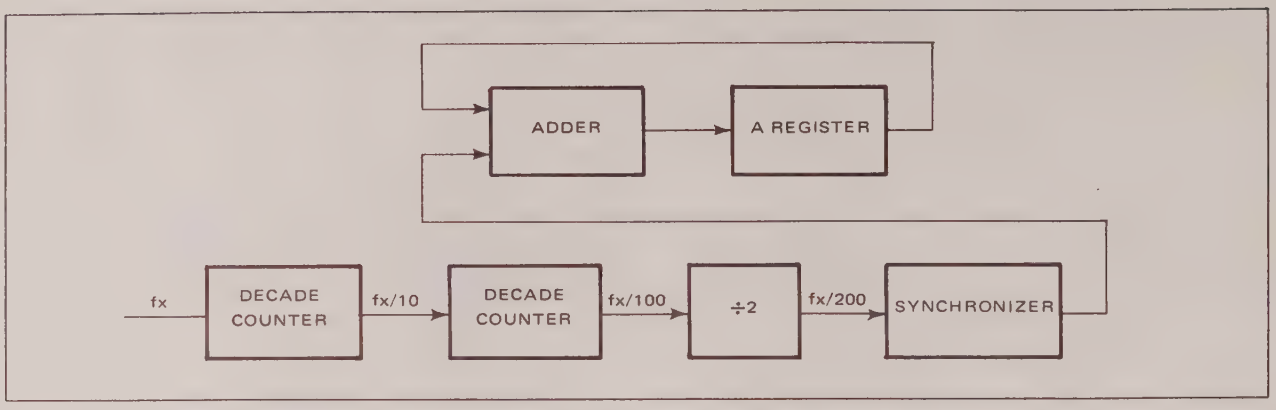


Figure 4.4 - Accumulator A, Simplified Block Diagram

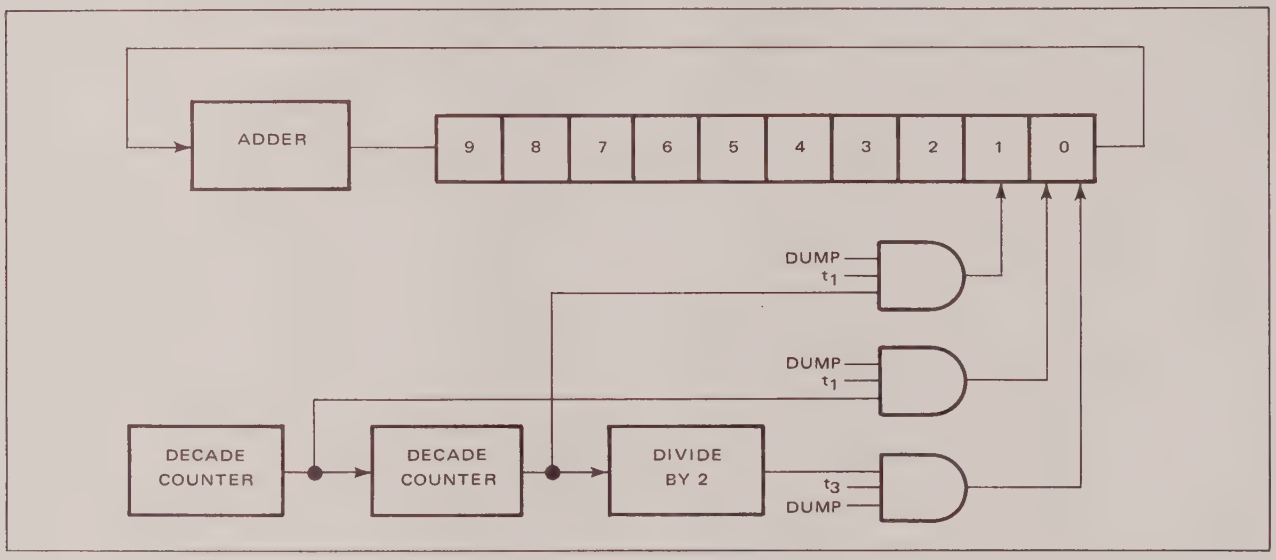


Figure 4.5 - Accumulator A Dump Logic

4.12 When the measurement time interval has been completed, the unknown frequency count must be divided by the time base count in order to obtain the final frequency data. Circulating registers are used as the accumulator registers in order to facilitate the arithmetic operations required to carry out the necessary division. The accumulated count word completes one circulation through the register and the associated adder every 2 microseconds. Thus counts can be accumulated at a maximum rate of 500 kHz. However, unknown frequencies up to 50 MHz must be counted. For this reason, a scale-of-200 counter is used ahead of the accumulator which is used to accumulate the unknown frequency count. (See figure 4.4.) This scale-of-200 counter consists of two decade counters and a divide-by-2 flip-flop. Each time that this counter recycles (that is, every 200 cycles of the unknown frequency), a count of 2 is added into the hundreds digit of the count being accumulated in the A-register. The synchronizer between the scale-of-200 counter and the A-register times the addition of the count to occur at the time in the accumulator circulation cycle when the hundreds digit of the count word is passing through the adder.

4.13 At the end of the measurement time interval, some portion of the total count resides in the scale-of-200 counter. Before the division process can begin, this count must be dumped into the A-register. The contents of the input decade counter is dumped into the units digit position of the accumulator count word. The contents of the second decade counter is dumped into the tens digit position. The contents of the divide-by-2 flip-flop is dumped into the hundreds digit position.

4.14 Figure 4.5 illustrates the technique used to dump the contents of the scale-of-200 counter into the A-register. In

this figure, the stages of the register are labelled 9 through 0. As the count word circulates through the register and adder, each digit resides for one clock period in each of the register stages. The designations of the stages indicate the digit which resides in each stage during the time period (t1) when the count word is lined up right in the register. During this period, the units (10^0) digit resides in the 0 stage, the tens (10^1) digit resides in the 1 stage, and so on. The transfer of the contents of the two decade counters to the A-register occurs during time t1 when the count word is lined up right in the A-register. This allows the contents of the input decade counter to be dumped into stage 0 while the contents of the second decade counter is dumped into stage 1. The adder does not have to be used to accomplish these transfers because the units and tens digits of the count word are 0's at this time.

4.15 The output of the divide-by-2 flip-flop is dumped into stage 0 of the A-register during clock period t3 when the hundreds digit of the count word resides in this stage. It might appear that the adder would have to be used for this transfer inasmuch as the hundreds digit of the accumulated count is not necessarily 0 at this time. However, the count is known to be even, since it represents the accumulation of a series of 2's entered via the adder each time that the scale-of-200 counter recycled. The data in each stage consists of a 4-bit BCD digit. Since the hundreds digit is known to be even, it follows that the 1-bit of the BCD code is known to be 0. Thus, a 1 can be transferred from the divide-by-2 flip-flop by setting the 1-bit of the stage to 1.

4.16 The B accumulator, where the time base count is accumulated, is similar to the A accumulator. However, in the case of the B accumulator, the frequency being counted is only 10 MHz. Thus, only a scale-of-100 counter (consisting of cascaded decade counters) is used ahead of the accumulator. Each time this counter recycles (that is every 100 counts of the 10 MHz), a 1 is entered into the hundreds digit of the B accumulator. At the end of the measurement period, the contents of the scale-of-100 counter is dumped into the units and tens digits of the count word held in the B accumulator.

4.17 Once the total unknown-frequency and time-base counts reside in the A and B accumulators, the division process can begin. The mechanization of division in the counter is very similar to the ordinary manual method of performing long division. This mechanization is simplified by the fact that the dividend is never more than 5 times as large as the divisor. This follows from the fact that the highest frequency that can be counted directly is 50 MHz while the reference count rate is 10 MHz. With this restriction in mind, consider the following manual long division routine:

```
        4.61
1284 ) 5921
       5136
        7850
        7704
         1460
         1284
          176
```

4.18 In performing this routine, quotient digits are determined one at a time in order of decreasing significance. In determining the first digit, 1284 is multiplied by various trial factors in order to find the largest resultant product which is smaller than or equal to 5921. The person performing the calculation may try 5 x 1284 = 6400. However, by inspection, this is larger than 5921. He may also try 3 x 1284 = 3852. However, when this is subtracted from 5921, a remainder of 2069 is obtained. Since this is larger than 1284, the trial product of 3852 is too small. When 4 x 1284 = 5136 is subtracted from 5921, a remainder of 785 is obtained. Since this is less than 1284, it is, indeed, the largest product that can be subtracted from 5921.

4.19 What has been determined to this point is that the largest product of the form 1284 X N that can be subtracted from 5921 without obtaining a negative difference is 1284 X 4. An equivalent statement is that the largest number of times that 1284 can be subtracted from 5921 without producing a negative balance is 4. This is an important equivalence because in the mechanized routine, successive subtractions are used in place of trial multiplications and subtractions.

4.20 In the mechanized routine, 1284 would actually be subtracted from 5921 five times. However, the fact that the fifth subtraction produces a negative difference would be sensed. This would cause the fifth subtraction to be cancelled by adding back 1284 to restore the balance to the positive difference, 785. The quotient digit is developed by counting the number of subtractions that result in a positive difference. In the example being considered, four such subtractions would be counted.

4.21 Successful completion of the search for the first digit leaves a remainder which is less than 1284. The second digit of the quotient is now found by determining how many times one-tenth of 1284 can be subtracted from the remainder. Actually, instead of using one-tenth of 1284, both the manual and mechanized routines use 10

times the remainder. In the mechanical routine, 10 times the remainder is formed by adding a 0 to the right of the least significant digit. Thus, remainder 785 becomes 7850. In the case of the mechanized routine, the remainder is multiplied by 10 by shifting it one place to the left in the A-register. Since the number held in the shift register is continuously circulating, the shift left is accomplished by inhibiting one clock pulse during a word cycle.

4.22 Once the remainder has been shifted left, the determination of the second digit of the quotient is implemented in the same manner as the determination of the first digit. In the example, the second digit is a 6 and a remainder of 146 is obtained. This remainder is then multiplied by 10 and the process is repeated in order to determine the third digit. (The determination of the third digit answers the question: how many times can 0.01 X 1284 be subtracted from the second remainder.)

4.23 After the determination that the third digit of the quotient is a 1, the manual routine is arbitrarily stopped although a third remainder has been found. When performing the manual routine, one may continue until a remainder of zero is produced or may stop after any arbitrary number of quotient digits have been determined. In the mechanized routine, ten quotient digits are calculated. This is actually one more than can be displayed even on a nine-digit unit. However, the extra calculation is necessary in connection with implementing the method of exit from the routine.

4.24 The first quotient digit is placed in the units position because it was determined by finding how many times 1 X 1284 could be subtracted from 5921. If the dividend had been 592.1, then the first quotient digit would have been determined by finding out how many times 0.1 X 1284 = 128.4 could be subtracted from 592.1. The first quotient digit would still be a 4, but now it would be to the right of the decimal point.

4.25 In the case of the manual routine, the calculator looks for a trial product of N X 1284 to subtract from 5921 because both numbers have four digits. Thus, the difference between a dividend of 5921 and a dividend of 592.1 would not change his procedure. However, he moves the decimal point from the dividend up into the quotient. Thus, the first quotient digit becomes 0.4 rather than 4. In the case of the mechanized routine, the manner which the dividend and divisor are lined up for subtraction is determined by their relative size. Thus, if 1284 is subtracted from 5921, a positive difference will be obtained. However, if 1284 is subtracted from 592.1, a negative difference will be obtained. After the negative balance is sensed, the routine adds back the divisor to restore the dividend to its initial value and then shifts the dividend to the left. Notice that in this case, a shift left has been implemented before any non-zero digit of the quotient has been developed. The routine takes account of this left shift by moving the decimal point one position to the left in the display.

4.26 The reference frequency count may be many times larger than the unknown frequency count. Thus, it may be necessary to shift the dividend to the left a number of times before a positive difference is obtained during a subtraction. Not every shift is accounted for by shifting the decimal point to the left. The decimal point is initially located to the right of the two most-significant digits at the start of the routine. After it has been shifted left two places, the next shift left of the dividend is accounted for by changing the units indicator by a factor of 1000 (from MHz to kHz) and shifting the decimal point two places to the right. This has a net affect of decreasing the significance of the most significant digit position by a factor of ten. The next two shifts are accounted for by shifting the decimal point to the left one place for each shift. The next shift is accounted for by changing the units indication from kHz to Hz and shifting the decimal point two places to the right. The next two shifts are accounted for by shifting the decimal point one place to the left for each shift. A total of 8 shifts of the dividend have been accounted for. If more shifts are required, then zeros are displayed in some of the digit positions in order to decrease the significance of the most-significant non-zero digit. To clarify the foregoing, the manner in which various frequency measurements in the frequency range from 500 MHz through 0.5 Hz would be displayed on a 9-digit display using a 10-second measurement time is presented in the following listing:

500.000000 MHz
50.0000000 MHz
5.00000000 MHz
500.000000 kHz
50.0000000 kHz
5.00000000 kHz
500.000000 Hz
50.0000000 Hz
5.00000000 Hz
0.50000000 Hz

4.27 Figure 4.6 illustrates in simplified form the functional organization of the hardware that is involved in the mechanization of the division routine. The A-register initially holds the dividend. As the routine progresses, it holds the shifted dividend or remainder. The B-register holds the divisor. These are both bit-parallel, digit-serial shift registers. The contents of both are continuously circulating. A complete word time requires 2 microseconds.

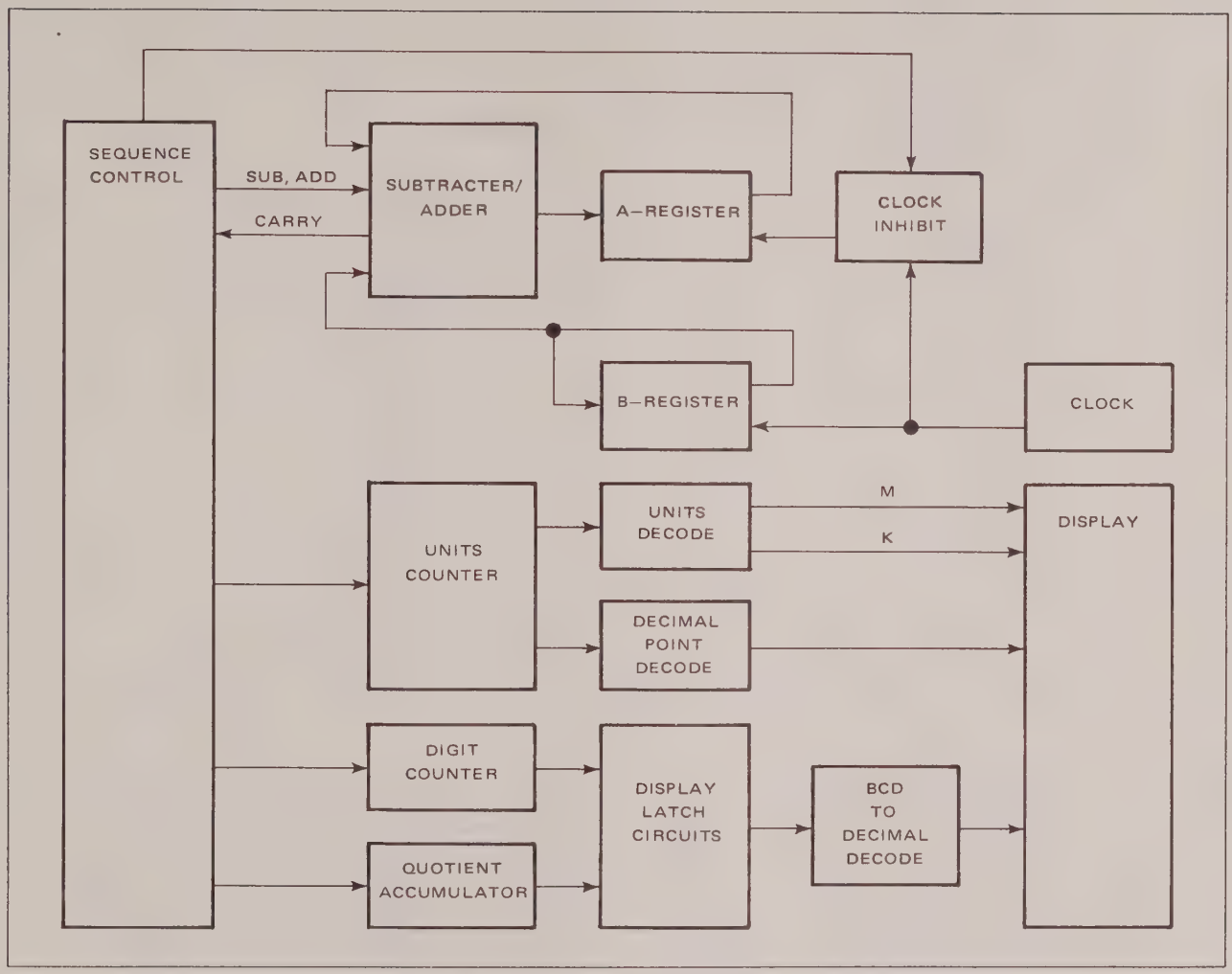


Figure 4.6 - Division Block Diagram

In this time, B may be either subtracted from or added to A. The determination of whether a subtraction or an addition occurs during any particular word time is controlled by the sequence control logic. For each subtraction that yields a positive or zero difference, the sequence control senses a carry out of the most-significant digit position. This indicates that another subtraction is in order. If a negative difference results from a subtraction, then no carry is sensed from the highest digit position. In this case, the sequence control provides an add-back (AB) during the next word time. Also, the contents of the A-register is shifted left one position by inhibiting the final shift pulse of the word cycle from reaching the A-register.

4.28 Three counters are used to keep track of the results of each step of the routine. The units counter is used to accumulate a count of the number of shifts of the dividend that occur before the first positive or zero difference is obtained. The status of the units counter is then decoded to determine the position of the decimal point and the particular units indication that is displayed.

4.29 After the dividend has been shifted 8 times or after the first positive difference has been obtained, the digits counter is incremented at the end of every add-back word time. The status of the digit counter determines the particular digit position in the display latch circuits in which any particular digit of the quotient is placed. The purpose of the digit counter, then, is to distribute the quotient digits from left to right in the display latches in the order in which they are determined.

4.30 The quotient accumulator is used to accumulate each quotient count. This accumulator is reset at the end of

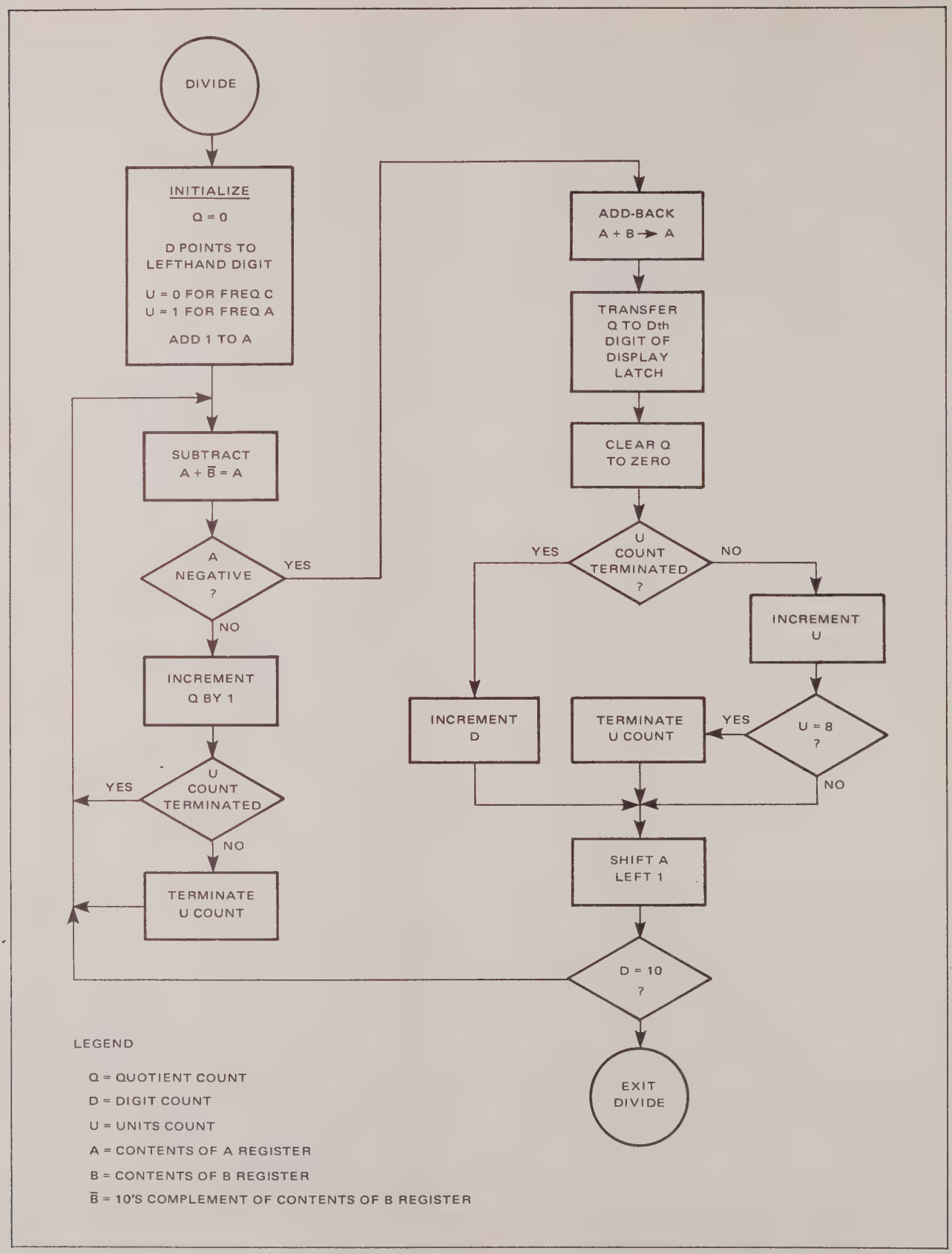


Figure 4.7 - Division Routine Flow Diagram

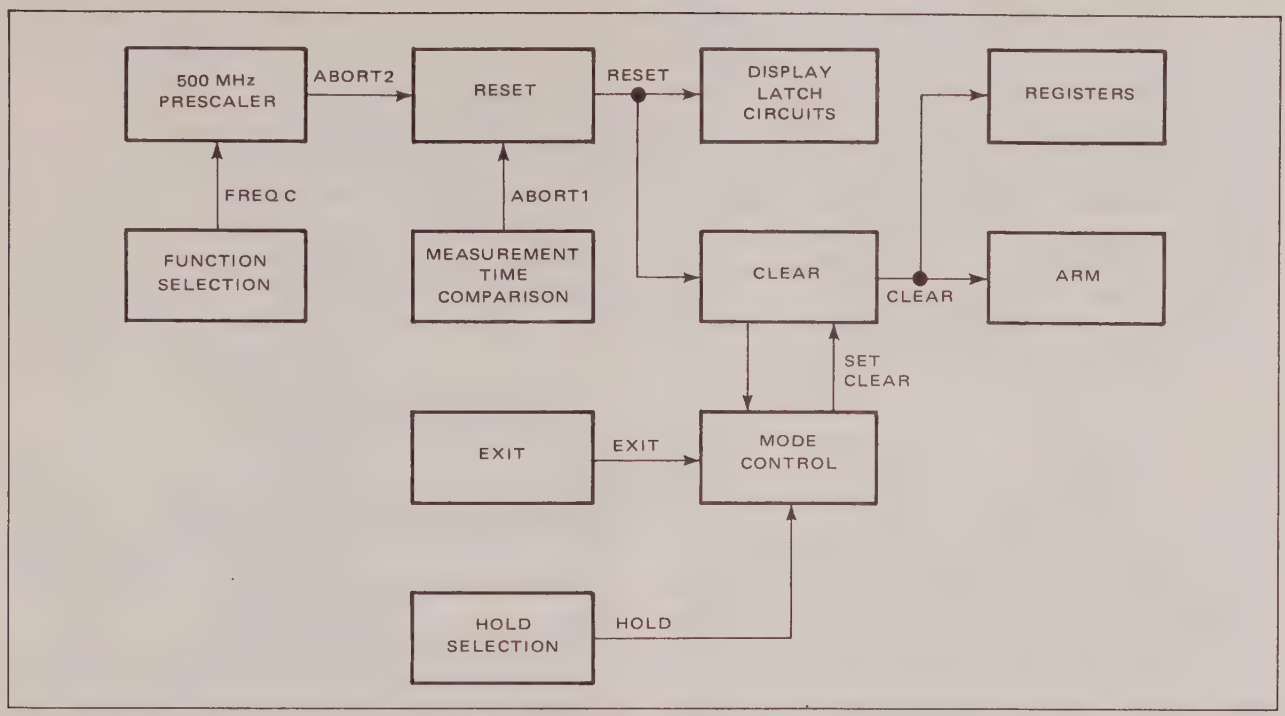


Figure 4.8 - Reset, Clear Block Diagram

each add-back word time and is incremented each time that a subtraction yields a positive or zero difference. Each time that an add-back occurs, the contents of the quotient accumulator are transferred into the display latch circuit being pointed to by the digit counter. (This even occurs before the first positive or zero difference has been obtained. In this case, the quotient value is zero and is always placed in the lefthand digit position inasmuch as the incrementing of the digit counter does not start until after the first positive or zero difference has been obtained.)

4.31 Figure 4.7 illustrates sequencing during a divide routine. Initially, the quotient count is reset to zero. The D count is set to point at the lefthand digit of the display. The setting depends upon the number of digits in the display (1 for 9 digits, 2 for 8 digits, and 3 for 7 digits).

4.32 When FREQ C is selected, the input frequency is divided by a factor of 10 in the prescaler. When FREQ A is selected, no such prescaling occurs. Thus, the divide routine for a 500 MHz input with FREQ C selected and the divide routine for a 50 MHz input with FREQ A selected will produce exactly identical sequences of subtractions and add-backs. Obviously, however, the decimal point must be positioned one place further to the left for the 50 MHz input than for the 500 MHz input. This is taken care of during the initialization period. At this time, U is set to 0 if FREQ C is selected and is set to 1 if FREQ A is selected.

4.33 If the dividend is several orders of magnitude larger than the divisor, the routine starts off with a number of subtract-add-back-shift A operations. During each of these operations, unless the U count has been terminated, U is incremented. The U count is terminated following the first subtraction that produces a positive or zero difference. Alternatively, if the U count reaches 8 before a positive or zero difference is obtained, then the U counting is terminated during a pass through add-back. In either case, once the U count has been terminated, each pass through add-back causes the digit count to be incremented.

4.34 The quotient count is reset to zero during each pass through add-back and is incremented each time that a positive or zero difference is obtained in a subtraction. During each pass through add-back, before the quotient counter is reset, the count held in it is transferred to the display latch in the digit position to which the digit counter is currently pointing.

4.35 The exit from the division routine marks the end of a complete frequency measurement cycle. At this time, the decision is made as to whether to rest or to start another measurement cycle. If the unit is in the HOLD mode, one measurement cycle is obtained in response to each actuation of the RESET switch. If the unit is in the AUTO mode, a continuous succession of measurement cycles is obtained. Figure 4.8 illustrates the logic that is involved in implementing the selected mode.

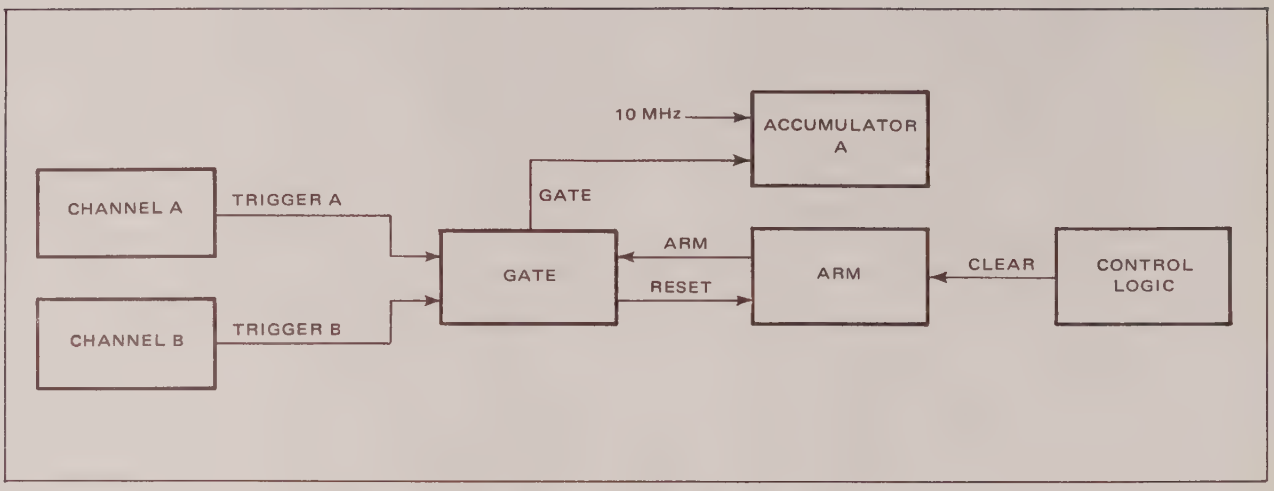


Figure 4.9 - Time Interval Counting Logic, Block Diagram

4.36 When the RESET switch is actuated or when a RESET pulse is generated by some other source, the display latches are reset so that the results of any previous measurement are cleared out of the display. The RESET pulse also sets the CLEAR signal. This signal clears the accumulator registers, initializes the control logic, and sets the ARM signal. Recall that the setting of the ARM signal enables the starting of a measurement time interval. Thus, each CLEAR cycle leads to another measurement cycle. When the division routine is completed, the EXIT signal is supplied to mode control logic. If the AUTO mode is selected, the mode control logic sets the CLEAR function in response to the EXIT signal. Thus, in this case, the end of one measurement cycle leads to the start of the next measurement cycle. If the HOLD mode is selected, the EXIT signal is inhibited from setting the control which sets the CLEAR function. Thus, in this case, the logic rests at the end of a measurement cycle. To obtain another measurement cycle in the HOLD mode, the RESET switch is again actuated.

4.37 Figure 4.8 illustrates two sources of the RESET signal other than the RESET switch. These are the measurement time comparison logic which supplies the ABORT1 signal and the 500 MHz prescaler which supplies the ABORT2 signal. The ABORT1 signal is supplied in the event that the time base count reaches 4 times the selected MEASUREMENT TIME before the gate signal is reset. This causes the measurement routine to be aborted if the unknown frequency signal being measured is lost or if the frequency of this signal is too low to be measured under the selected conditions. The ABORT2 signal can be supplied only if the 500 MHz prescaler is in use as indicated by the FREQ C function selection signal being true. In this case, it is supplied if the input signal level is too high or too low to insure accurate frequency measurement.

4.38 TIME INTERVAL MEASUREMENT.

4.39 The time interval measurement is accomplished by accumulating a count of the cycles of the 10 MHz time base signal during the interval of interest. The start of the interval is defined by the signal being applied to the channel A 50-MHz trigger amplifier while the termination of the interval is defined by the signal being applied to the channel-B 50-MHz amplifier. (See figure 4.9.) As in the case of frequency measurement, the measurement is initiated by the setting of the ARM signal in response to the trailing edge of the CLEAR signal. With the ARM signal true, the next true-going transition of the TRIGGER A signal sets the GATE signal as required to enable the accumulation of the count.

4.40 In the case of the time interval measurement, the ARM signal is reset when the GATE signal sets. The GATE signal is now reset by the next false-going transition of the TRIGGER B signal from channel B.

4.41 At the end of the measurement of the time interval, the contents of the scale-of-200 counter is dumped into the accumulator as in the frequency measurement routine. With the complete time interval count held in the A-register, it remains only to transfer this count into the display latch circuits. (The count represents a count of 0.1 second periods. It is displayed as microseconds with the decimal point to the left of the least-significant digit. Thus, the accumulated count can be used directly as the display data.) The transfer of each digit of the count to the appropriate stage of the display latch circuits is implemented by applying the A-register outputs to a display data bus and then clocking the digit appearing on the bus during each successive clock period into the appropriate display latch stage. (See figure 4.10.)

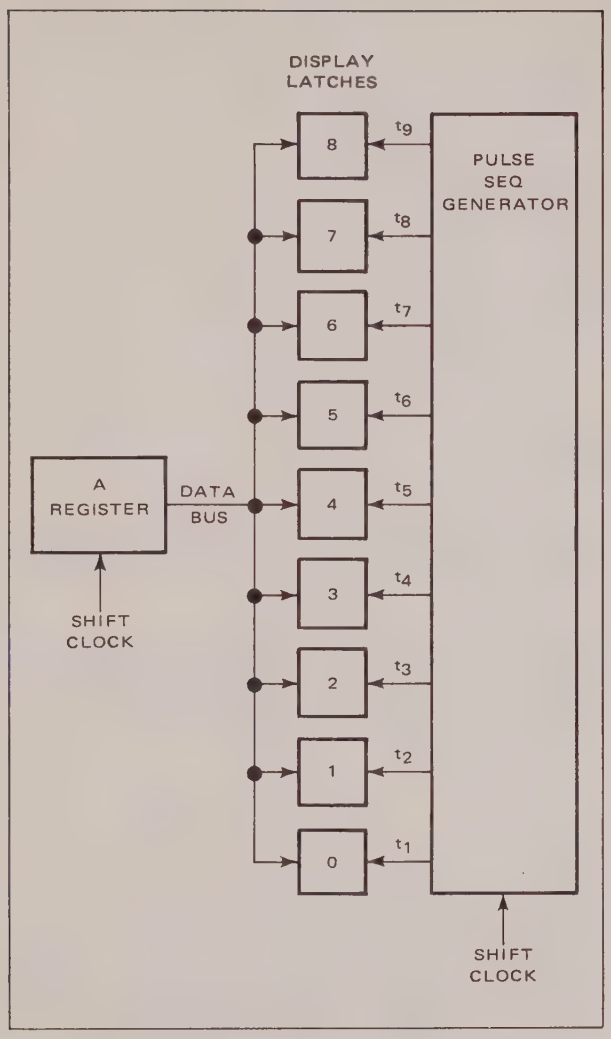


Figure 4.10 - Time Interval Count Transfer

4.42 After the transfer of the time interval count, the unit times out the selected MEASUREMENT TIME count. This is accomplished using the B accumulator and the time base comparison logic as described for the frequency measurement routine. However, in the case of the time interval measurement routine, the purpose of timing out the selected MEASUREMENT TIME count is to introduce a delay between the completion of the time interval measurement and the decision as to whether or not to start another measurement cycle. Thus, if the unit is operating in the AUTO mode, the MEASUREMENT TIME selection determines the length of the interval between successive measurement cycles.

4.43 DETAILED CIRCUIT ANALYSIS.

4.44 The remainder of this section provides a detailed description of the theory of operation of logic circuits and analog circuits with reference to the logic and schematic diagrams contained in Section 8. For convenience in referring to the drawings the organization of the text follows the organization of the drawings.

4.45 External Reference Processing Circuit and Reference Selection Logic.

4.46 Refer to figure 4.11 for a block diagram of the external reference processing circuit and reference selection logic. Refer to drawing 721046, sheet 1 for the schematic and logic diagram.

4.47 An external reference input from the EXT REF connector is applied to buffer amplifier Q1. The frequency of this input must be 1 MHz, 2.5 MHz, 5 MHz, or 10 MHz. The output of Q1 is applied to Schmitt trigger Q3-Q4. This converts the input waveform into a square wave as required

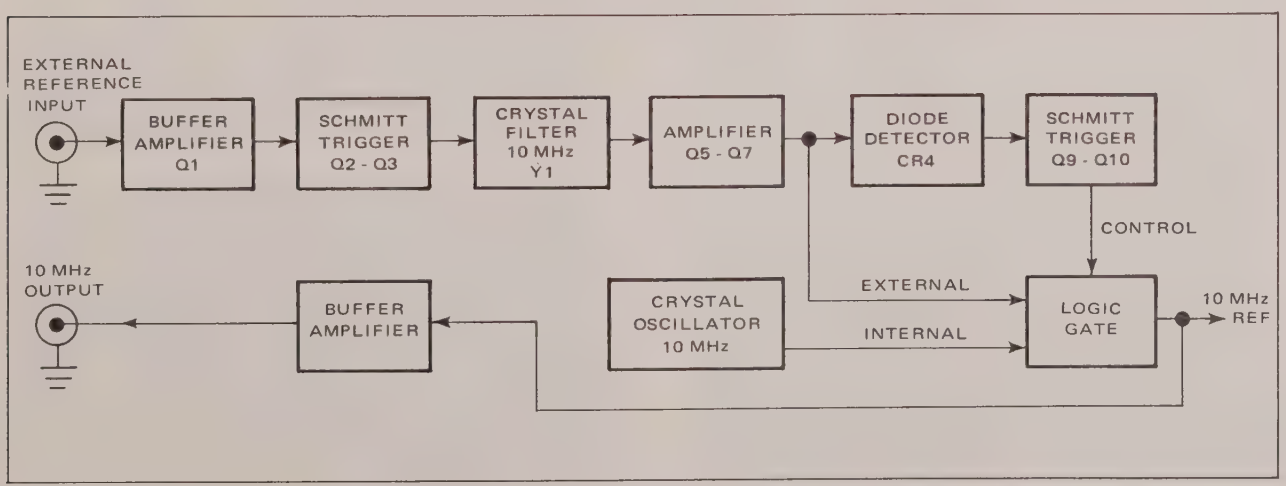


Figure 4.11 - External Reference Processing Circuit and Reference Selection Logic

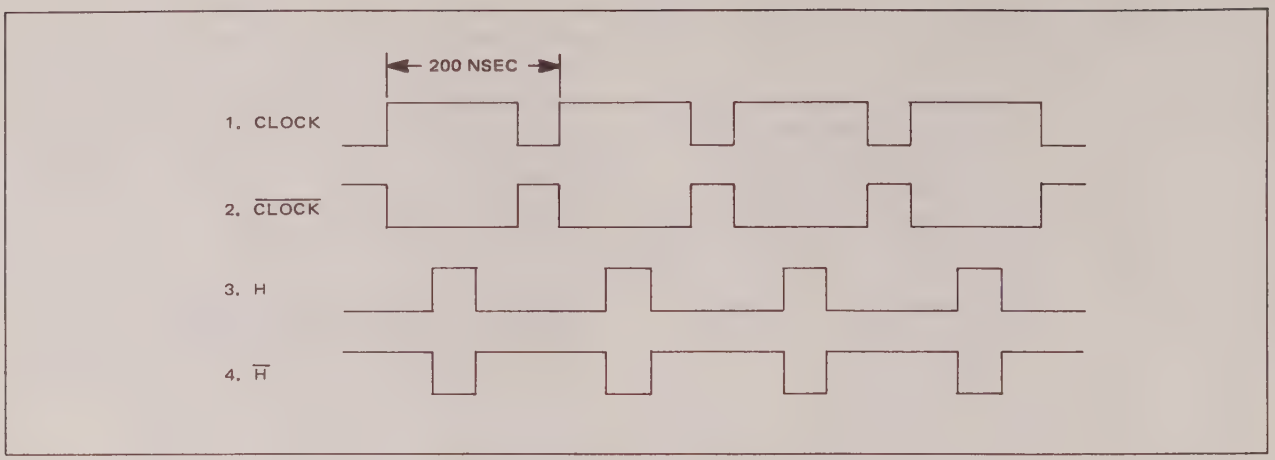


Figure 4.12 - Clock and H Signal Timing

to obtain harmonics of the input frequency. Crystal filter Y1 rejects frequency components other than 10 MHz and passes 10 MHz signals to amplifier stage Q5. Amplifier stages Q5 through Q8 provide amplification of the 10 MHz signal which is supplied from the output of Q8 to a gate in the reference frequency selection logic.

4.48 The status of the reference selection logic is determined by the status of Schmitt trigger Q9-Q10. This Schmitt trigger is controlled by the output from a diode detector which provides positive peak detection of the 10 MHz signal at the collector of Q6. The output from Q6 is coupled through capacitor C15 to a DC restorer circuit employing diodes CR5 and CR6. This circuit clamps negative peaks of the signal from Q6 to ground potential. The anode of CR6 is held one diode drop above ground to compensate for the negative voltage drop through CR5. The signal from the DC restorer is peak-detected by diode CR4 and capacitor C18. When the 10 MHz signal at Q6 reaches a level indicating that the amplified external reference voltage is large enough to operate the counter, Q9 is turned on and Q10 is cut off. With Q10 cut off, a positive-true level is supplied to NAND gate MA5-11 which also receives the 10 MHz signal from amplifier Q8. Thus, under this condition, this signal is gated to the 10 MHz REF line and is used as the reference frequency signal for the counter.

4.49 The positive-true signal from Q10 is inverted by NAND gate MA5-3 to inhibit NAND gate MA5-6 which receives the 10 MHz signal from the internal oscillator. Thus, under this condition, this signal is not used.

4.50 When an external reference input is not being supplied or is below the required level, then the status of Schmitt trigger Q9-Q10 is reversed. Q10 now conducts and inhibits NAND gate MA5-11. Under this condition, NAND gate MA5-6 is enabled and the 10 MHz signal from the internal oscillator is supplied to the 10 MHz REF line.

4.51 In addition to being used internally, the selected 10 MHz signal is applied through continuously-enabled NAND gate MB5-11 and capacitor C21 to the 10 MHz OUT line to the 10 MHz OUTPUT connector on the rear of the unit.

4.52 Clock, Bit, and Word Timing Logic.

4.53 Flip-flop MA6-9 divides the 10 MHz REF signal by 2 to provide a 5 MHz rate which serves as the reference for bit and word timing. The two outputs of flip-flop MA6-9 are gated with the 10 MHz REF signal to produce the two clock signals $\overline{\text{CLOCK}}$ and H and their complements. The phase relationships of these signals are illustrated in figure 4.12.

4.54 Positive-going transitions of the CLOCK signal are used to clock a 10-stage ring counter whose outputs define the 10 bit periods of a word period. The timing of the bit period signals (t1 through t10) is illustrated in figure 4.13.

4.55 The ring counter employs two 5-bit shift registers (MB10 and MB9) operated in cascade to form a 10-bit shift register. The ring count mode is enforced by decoding the zero status of the first nine stages of the shift register and using this decode as the serial input to the shift register. This provides start-up from any arbitrary status. Any 1's initial residing in the shift register are shifted to the right until the first nine stages contain all zeros. A 1 is then shifted into the input of the shift register in response to the next shift pulse.

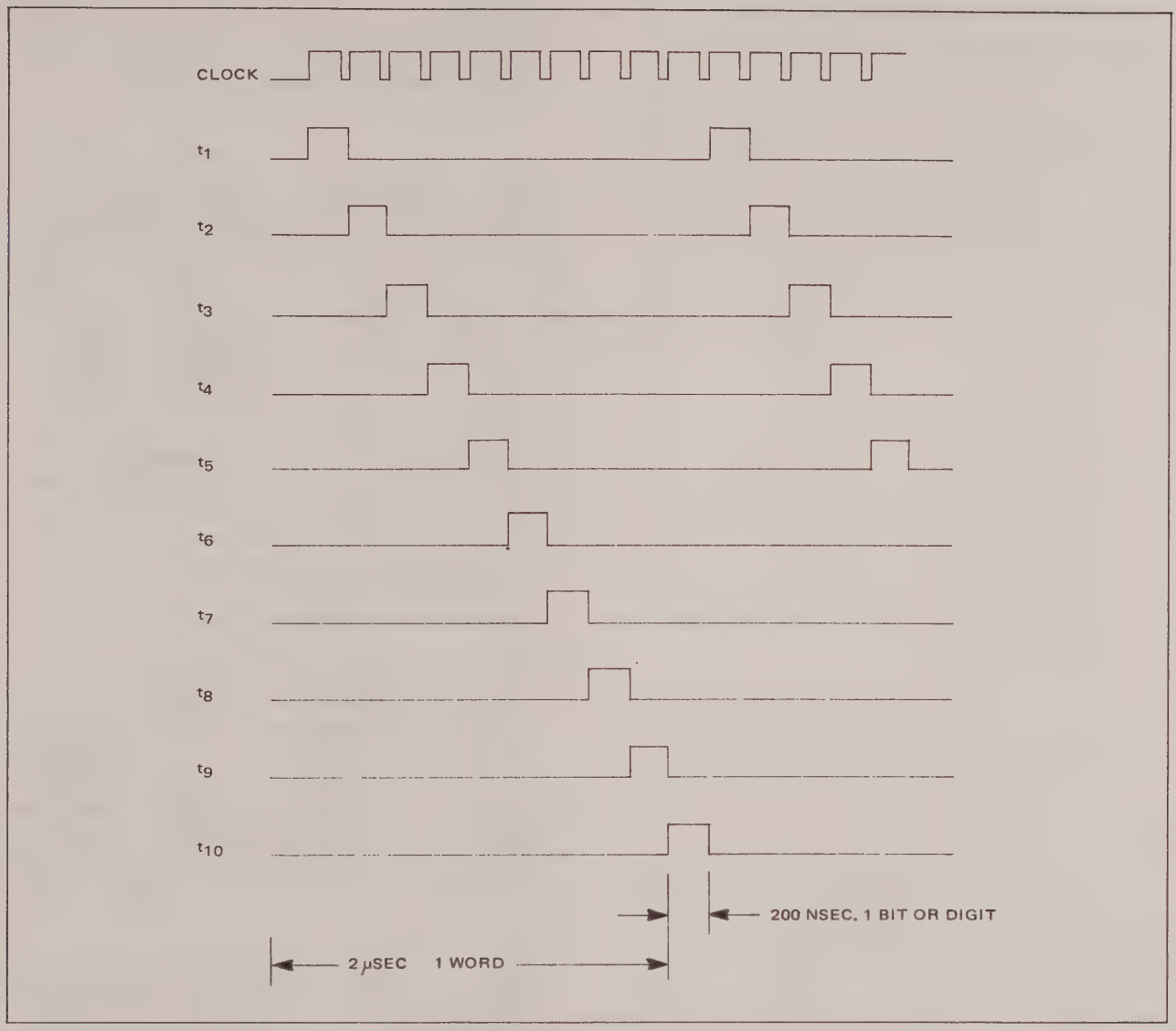


Figure 4.13 - Ring Counter Waveforms

4.56 Digit Counter.

4.57 The digit counter employs two 5-bit shift registers (MB7 and MB8) operated in cascade to form a 10-bit shift register. The preset capabilities of the shift register modules are used to select an initial digit status appropriate to the number of digits in the display. In the case of a 9-digit display, the D1 through D9 signals are used to enable the sequential loading of quotient digits into the display latches associated with the 9 digit positions in order of decreasing significance. In the case of an 8-digit display, only the D2 through D9 signals are used and in the case of a 7-digit display only the D3 through D9 signals are used. When the register is preset, a binary 1 is entered into the stage associated with the first signal being used (D1, D2, or D3). Jumpers are used to condition the logic for the initialization appropriate to the number of digits being used.

4.58 Prior to being preset, the shift register must first be reset to the all-zero condition. This is accomplished in response to the $\overline{\text{CLEAR}}$ signal that is received from the sequence control logic at the end of each frequency measurement sequence or time interval measurement sequence or in response to a unit reset pulse. The presetting of the digit

count then occurs in response to the $\overline{Z}$ pulse which is received during bit period t3 of the initiate-word time of the division sequence of a frequence measurement sequence.

4.59 The digit count shift register is clocked by each INC D pulse that is received from the sequence control logic during the division sequence. An INC D pulse is received during each add-back word time following the accumulation of a particular quotient digit. Thus, as each successive quotient digit is accumulated, the digit count points to another digit position of the display storage latch logic as required to load successive quotient digits into successively lower order digit positions in the display latch logic.

4.60 Display Logic.

4.61 The reference drawing sheet illustrates the following logic:

a. The latch circuits used to store BCD data for each of the nine possible display digit positions.

b. The BCD-to-decimal decoder-drivers used to convert the stored data to decimal form and to drive the display tube elements.

c. Gates via which digit data is loaded into the BCD latch circuits and associated control logic.

d. A decade counter used to accumulate digit counts during the divide routine.

4.62 The latch circuits employ nine SN7475 4-bit bistable latch circuits all of which receive data inputs from a common 4-bit data bus. At any particular digit entry time, only one of the latch circuits receives the positive clock pulse required to strobe the data from the common bus into the latch circuit.

4.63 Data is applied to the latch circuit data input bus via four NAND gates which receive data from either one of two sources. One source is the A-register in the high speed-switching logic. The A-register outputs (A1-8, A1-4, A1-2, and A1-1) are gated to the latch circuit data input bus by a false $\overline{\text{TI TRNF}}$ level from the time-interval measurement sequence control logic. The $\overline{\text{TI TRNF}}$ signal becomes false for one word time during a time-interval measurement sequence when the time interval data is available in the A-register. During this word time, as each digit of the time interval data resides in the output stage of the A-register, it is copied into the appropriate digit position in the display latch circuits. This is implemented in response to clock pulses from a group of nine gates each of which receives a different bit timing signal. All nine of these gates receive a signal from NOR gate MC6-13 which accepts the $\overline{H}$ and $\overline{\text{TI TRNF}}$ signals. As a result, at H time of each bit period, the appropriate latch circuit receives a clock pulse. Thus, during the first nine bit periods of the word period, the digits in order of increasing significance are copied in sequence into the nine display latch circuits.

4.64 The second source of data for the display latch circuits is decade counter MB3 which is used to accumulate each quotient digit during the division routine of a frequency measurement sequence. The outputs of this counter are applied to the display latch input data bus at bit time t3 of each add-back (AB) word time. The fact that an add-back is in progress indicates that the computation of a particular quotient digit has been completed. The particular digit position into which the digit data is loaded is determined by the status of the digit count shift register. When D1 from the digit count shift register is true, the display latch associated with the most significant digit position is clocked at t3 time of AB time and thus the digit data from the decade counter is stored in the most-significant digit latch. Similarly, each succeeding Dx signal enables a clock pulse to a less significant digit latch as required to load quotient digits in order of decreasing significance which is the order in which they are generated by the divide routine.

4.65 The decade counter is reset in response to the Z signal received during t3 time of the initialize word time of a frequency measurement sequence from the sequence control logic. The decade counter is also reset by each F pulse from the sequence control logic. An F pulse is received each time either the units count or the digit count is incremented. Either of these events indicates that the generation of a particular digit has been completed. The counter is thus reset in preparation for the accumulation of the next digit.

4.66 The count signal accumulated by the decade counter is the INC Q signal from the sequence control logic. An INC Q pulse is received each time that a subtraction yields a positive difference.

4.67 When a $\overline{\text{RESET}}$ pulse is received, it is applied to the clock lines of all nine display latch circuits. Since the display latch data input bus lines are all at the false level during the $\overline{\text{RESET}}$ pulse time, all of the display latches are reset to the zero status.

4.68 $\overline{\text{PRINT}}$ Gate.

4.69 Gate MB6-3 holds the $\overline{\text{PRINT}}$ line at the true level when either $\overline{\text{DIV}}$ or $\overline{\text{TI TRNF}}$ is false. A false DIV signal indicates that the contents of the display latches is in the process of being modified by a divide routine which is currently in progress. A false $\overline{\text{TI TRNF}}$ signal indicates that new time interval data is currently being copied into the

display latches. Thus, in either case, the latch outputs are not currently valid and should not be strobed to an external printer.

4.70 AUTO Gate.

4.71 Gate MD6-4 supplies the AUTO signal to the electrical outputs logic for application to external equipment. This signal is held false when the HOLD signal from the mode selection logic is true, indicating that the unit is in the HOLD mode. It is also held false when the $\overline{\text{RESET}}$ signal is false. This corresponds to the fact that the unit is essentially in the HOLD status during reset.

4.72 Units Counter and Decoder and Associated Driver Logic.

4.73 During frequency measurement operation, the status of the units counter determines the status of the units display and the position in which the decimal point is displayed. The units counter is decade counter MC5. Its BCD outputs are made available for external use at pins of edge connector J9 and are also supplied to BCD-to-decimal decoder MC4. The decimal outputs of the decoder are distributed to five NAND gates which are used here to provide OR functions. Two of these NAND gates control respectively the drivers for the M and K lamps. The remaining three drivers control respectively the drivers associated with the DP-B, DP-C, and DP-D decimal point drive signals. Each of these decimal point drive signals lights a decimal point in a different position of the display.

4.74 During frequency measurement operation, the TI signal from the mode selection logic is false. Under this condition, Q22, which is the driver for the Hz display lamp is continuously enabled to conduct so that Hz is continuously displayed. Depending upon the status of the units counter, M or K may also be lighted so that the units display may be MHz, kHz, or Hz.

4.75 When a particular decimal decode output from MC4 becomes negative-true, the outputs of any of the NAND gates to which it is applied become true. This causes the driver transistors associated with the NAND gates to conduct and turn on the associated units display or decimal point display. For example, when the 0 decode output from pin 1 of MC4 becomes low, the outputs of NAND gates MC3-12 and MC3-6 become true. This causes transistors Q20 and Q15 to conduct. With Q20 conducting, the M lamp is turned on so that MHz is displayed. With Q15 conducting, the decimal point display is turned on in the display tube which receives the DP-B signal.

4.76 The signals from the decimal decoder are distributed so that MHz is displayed when the units count is 0, 1, or 2; kHz is displayed when the units count is 3, 4, or 5; and Hz is displayed when the units count is 6, 7, or 8. Associated with each of these units displays are three possible positions of the decimal point. These provide, respectively 1, 2, or 3 digits to the left of the decimal point. The position of the decimal point and the units display for each of the possible states of the units counter is summarized below for a 9-digit display:

Units Count	Display Status
0	123.456789 MHz
1	12.3456789 MHz
2	1.23456789 MHz
3	123.456789 kHz
4	12.3456789 kHz
5	1.23456789 kHz
6	123.456789 Hz
7	12.3456789 Hz
8	1.23456789 Hz

4.77 At the start of each computation cycle, the units counter is reset by the $\overline{Z}$ signal which is received at t3 time of the initiate word time from the sequence control logic.

4.78 If the FREQ A signal from the mode selection logic is true, indicating that the frequency being measured is not being pre-scaled, then the units counter is clocked at t9 time of the initiate (INT) word time. This advances the units count to 1. This establishes the initial condition in which there are two digits to the left of the decimal point and MHz is displayed. This prepares for the display of the maximum frequency (50 MHz) that can be measured without using the pre-scaler. If FREQ A is false, then the units count is not incremented during the initiate word time and the units count remains at 0. This prepares for the display of the maximum frequency (500 MHz) that can be measured using the pre-scaler.

4.79 During the first part of the computation routine before the first positive difference has been obtained from the computation of A - B, an INC U pulse is received from the sequence control logic for each time that a negative difference is obtained and the restored contents of A is shifted to the left. Each such INC U pulse increments the units count. Therefore, the final status of the units count at the end of this portion of the computation routine is determined by the number of times that the restored contents of A must be shifted left before a positive difference is obtained.

4.80 During time interval operation, the TI signal from the mode control logic is true. This jams the counter in the 9-count status. Since the 9 output of the BCD-to-decimal decoder is not distributed to any of the associated NAND gates, none of the drivers used in the frequency measurement mode is selected. The true TI level turns on driver Q18 as required to illuminate the USEC lamps. With Q18 conducting, the DP-A line is also pulled to the active level causing the decimal point located to the left of the least significant digit of the display to light. The resultant status for a 9-digit display is as follows:

12345678.9 USEC

4.81 Digit Blanking Logic.

4.82 The resolution of the measurement time count is 100 ns. Thus, the precision that can be achieved in a frequency measurement depends upon the length of the measurement time interval. When the maximum interval of 10 seconds is selected, a precision of 1 part in 10^8 (nine decimal digits) is achieved. For a 1 second measurement time, the precision drops to 1 part in 10^7 (8 decimal digits). For a 0.1 second measurement time, the precision drops to 1 part in 10^6 (7 decimal digits). The purpose of the digit blanking signals is to blank out the display of those digits which are not significant for the particular precision being achieved. In the case of the selection of the 10 second interval, all nine digits are required and no blanking signal is generated. When a 1 second interval is selected, the 1 signal from the signal conditioning logic becomes true. This is applied through steering diode CR7 to the base of transistor Q11. This causes Q11 to conduct and place the BLANKING 1 line at the low level. With the BLANKING 1 line at the low level, the righthand display tube is blanked.

4.83 When a 0.1 second interval is selected, the .1 signal from the signal conditioning logic becomes true. This is applied through steering diodes CR8 and CR11 to the base circuits of transistors Q11 and Q12. In this case, both the BLANKING 1 and the BLANKING 2 lines are placed at the low level and the two righthand display tubes are blanked.

4.84 In a similar manner, each progressively shorter measurement time interval selection causes an additional blanking signal to be placed at the low level so that one additional display tube is blanked.

4.85 The measurement time selection signals received from the signal conditioning logic are gated by the TI signal. Thus, blanking is inhibited when the unit is operating in the time-interval measurement (TI) mode.

4.86 Unknown Frequency Selection Gates and Count Gate.

4.87 There are two sources of the unknown frequency signal, FX:

a. When the FREQ C signal from the signal conditioning logic is false; that is, when FREQ A is selected; the TRIGGER A signal from the 50 MHz preamplifier is gated to the F_X line via NOR gate MK7-10.

b. When $\overline{\text{FREQ C}}$ is false; that is, when FREQ C is selected; the TRIGGER C signal from the 500 MHz pre-scaler is gated to the F_X line via NOR gate MK7-9.

4.88 F_X is supplied to the sequence control logic where it is used in connection with both initiating and ending the frequency measurement time interval. During the frequency measurement time interval, F_X is supplied via NOR gate MK7-4 to the input (MJ7-6) of the high-speed decade counter associated with accumulator A as required to accumulate a count of cycles of the unknown frequency. F_X is applied to NOR gate MK7-4 through NOR gate MK6-6 which is enabled during frequency measurement operation by the false TI level from the mode control logic. The passage of F_X through NOR gate MK7-4 is enabled by false levels from NOR gate ML5-13 and a false $\overline{\Delta t_M}$ signal from the sequence control logic. The output of NOR gate ML5-13 is held continuously false during a frequency measurement operation by the true $\overline{\text{TI}}$ level from the mode control logic. The $\overline{\Delta t_M}$ signal is true when the frequency measurement time interval is in progress.

4.89 During an interval timing operation, the F_X signal is inhibited from reaching NOR gate MK7-4 because the output of NOR gate MK6-6 is held continuously false by the true TI level. Under this condition, it is the signal from NOR gate ML5-13 which is gated through NOR gate MK7-4 by the false $\overline{\Delta t_M}$ level. NOR gate ML5-13 is enabled by the false $\overline{\text{TI}}$ level to pass the 10 MHz REF signal from the reference frequency logic.

4.90 End-Abort Logic.

4.91 The $\overline{\text{END}}$ signal is supplied when the count accumulated in register B corresponds to the selected MEASUREMENT TIME. Since the available measurement time selections are 10 seconds, .1 second, 0.1 second, 0.01 second, and 0.001 second; the accumulation of the required count can be sensed by monitoring the bit 1 output of the B-register during the appropriate bit period. Every count

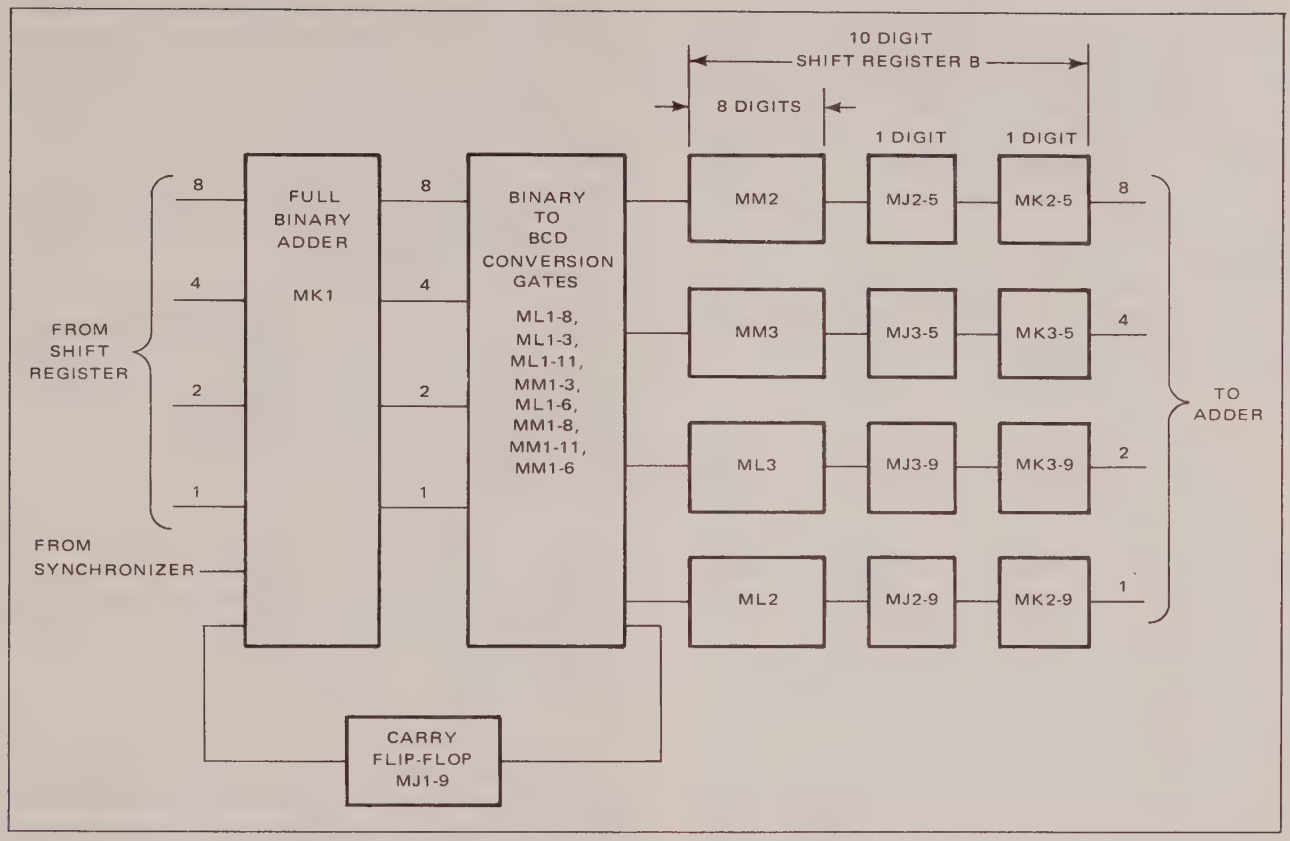


Figure 4.14 - Accumulator B, Block Diagram

accumulated in the B-register corresponds to a time interval of 0.1 μsec. Thus, the selected measurement time of 0.001 second corresponds to a B-register count of 10,000. In order to sense this count, it is necessary to monitor for a true bit 1 in the 5th digit position of the measurement count word. This digit is available in the output stage of the B-register during bit period t5 of each word time. Thus, a binary 1 appearing in bit position 1 at the output of the B-register during t5 time must place the $\overline{\text{END}}$ signal at the false (active) level, if the selected MEASUREMENT TIME is 0.001 second.

4.92 The signal which times the monitoring of the bit 1 position of the B-register output is the TB signal from the time base gates (sheet 3). This signal is true during the particular bit period of each word time which is appropriate for sensing the completion of the selected MEASUREMENT TIME count. (In the case of the 0.001 second selection, TB is true during t5 time.) TB is gated to the line controlling one input of the $\overline{\text{END}}$ and $\overline{\text{ABORT}}$ gates by the $\overline{\text{TI}}$ signal from the mode control logic. This signal is continuously true when the unit is in the frequency measurement mode.

4.93 If the bit 1 output of the B-register is true during the bit time when TB is true, then the $\overline{\text{END}}$ signal is placed at the false level during this bit period. The false $\overline{\text{END}}$ signal resets a control flip-flop in the sequence control logic. This prepares for the termination of the measurement time interval in response to the next true-going transition of the unknown frequency signal.

4.94 The measurement time count continues to accumulate between the time that the completion of the selected MEASUREMENT TIME is sensed and the next true-going transition of the unknown frequency signal. If the measurement time count reaches 4 times the selected value, then an abort occurs. The $\overline{\text{ABORT1}}$ signal occurs if the bit 4 output of the B-register is true during the period when TB is true. (In the case of a selected MEASUREMENT TIME of 0.001 second, this would indicate that the accumulated count had reached 40,000 that is, 4 times the selected count of 10,000.)

4.95 The $\overline{\text{ABORT1}}$ signal is supplied to the sequence control logic where it causes the generation of a CLEAR pulse and a RESET pulse. The CLEAR pulse terminates the measurement sequence and the RESET pulse resets the display latches so that an all-zero reading is obtained.

4.96 Accumulator B.

4.97 For the purpose of this discussion, accumulator B is defined to include the components shown in figure 4.14.

The 4-bit by 10-digit shift register employs flip-flops for the two righthand digit positions and employs 8-bit shift registers for the 8 lefthand bit positions. The 10-digit measurement time count word circulates through the shift register and the adder once during each word time. During bit period t1 of each word time, the least significant (units) digit of the word resides in the righthand digit position of the shift register and is presented to the A inputs of the adder. During bit period t2, it is the tens digit which occupies this position. During bit period t3, it is the hundreds digit. If there is a carry from the two decade counters into the accumulator, it is supplied from the synchronizer during bit period t3. It is thus added to the hundreds digit of the measurement time count word.

4.98 At the start of measurement time, the shift register is reset. Each successive carry from the decade counters is accumulated in the hundreds digit of the time word count as it is added to the previous balance by the adder. As long as the adder output is within the range of 0 to 9, it passes through the binary-to-BCD conversion gates without modification. When the tenth count pulse is received from the synchronizer, the adder output increases to 1010 (decimal 10). This status is decoded by the binary-to-BCD converter gates and is converted into a 0000 digit for application to the shift register input and a binary 1 carry for application to the CARRY flip-flop. At the time that the 0000 digit is clocked into the shift register, the CARRY flip-flop is set. During the next bit period, this binary 1 CARRY bit is added into the thousands digit of the measurement time count word and the CARRY Flip-flop is reset.

4.99 Notice that because counts are received one at a time from the synchronizer, the maximum sum output from the binary adder is 10. Thus, this is the only value that requires conversion from binary form into a BCD sum and carry component. Propagation of carries into higher orders of the measurement count word occurs in the same manner as just described for the propagation of the carry from the hundreds order into the thousands order.

4.100 At the end of the measurement time interval, the units and tens digits of the measurement count word held in the shift register remain at the initial zero value since no entries have occurred into these digit positions. At this time, the units and tens digits of the final count reside in the two decade counters. These counts are now transferred into the units and tens digits positions of the measurement count word in the shift register. This occurs during t1 time when the units and tens digits are located in the two righthand digit positions in the shift register. Because, the units and tens digits are known to be zeros before the transfer, the transfer can be accomplished by using the binary 1's of the counts held in the decade counters to direct set the associated bit flip-flops of the shift register.

4.101 The tens digit data is obtained from decade counter MJ5 while the units digit data is obtained from decade counter MK5. The positive-true bit outputs of these decade counters are applied to the direct set inputs of the shift register flip-flops through eight NAND gates which invert the binary 1's to negative signals as required to direct set the flip-flops. The control inputs to the eight gates are controlled by two NOR gates which receive the $\overline{t1}$ signal and the $\overline{DUMP \cdot H}$ signal from NAND gate MD4-11 (shown on sheet 2 of drawing 721081).

4.102 The $\overline{t1}$ signal times the transfer to occur during bit period t1 of the word time when the accumulated measurement time count word is positioned with its tens and units digits in the two righthand digit positions of the shift register. The $\overline{DUMP \cdot H}$ signal times the signal to occur at the end of the measurement time.

4.103 The shift register and the CARRY flip-flop are clocked continuously at the bit rate by the CLOCK signal from the timing logic on the readout board. A group of continuously enabled gates provides a fanout of the CLOCK signal as required to obtain the drive for all components of the shift register.

4.104 The shift register elements and the CARRY flip-flop are reset at the start of the measurement time by the CLEAR signal from the sequence control logic. This signal is inverted and supplied to the shift register reset inputs by two NOR gates used as inverting drivers.

4.105 Measurement Time Decade Counters and Synchronizer.

4.106 Two decade counters operated in cascade provide modulo-100 counting of the 10 MHz REF signal during the measurement time. Each carry out of the modulo-100 counter is accepted by the synchronizer and held until t3 time when it is added into the hundreds digit of the measurement time count word being accumulated in register B as described in paragraph 4.97.

4.107 The 10 MHz REF signal is gated to the input of decade counter MK5 during measurement time. The most significant bit output of this counter is applied to the input of decade counter MJ5. The counts are incremented in response to a false-going transition. Thus, as counter MK5 recycles to zero, the count held in counter MJ5 is incremented.

4.108 The most significant bit output of counter MJ5 is applied through a NOR gate to the clock input of flip-flop MG5-9 of the synchronizer. When the two decade counters recycle to zero together at the end of 100 counts,

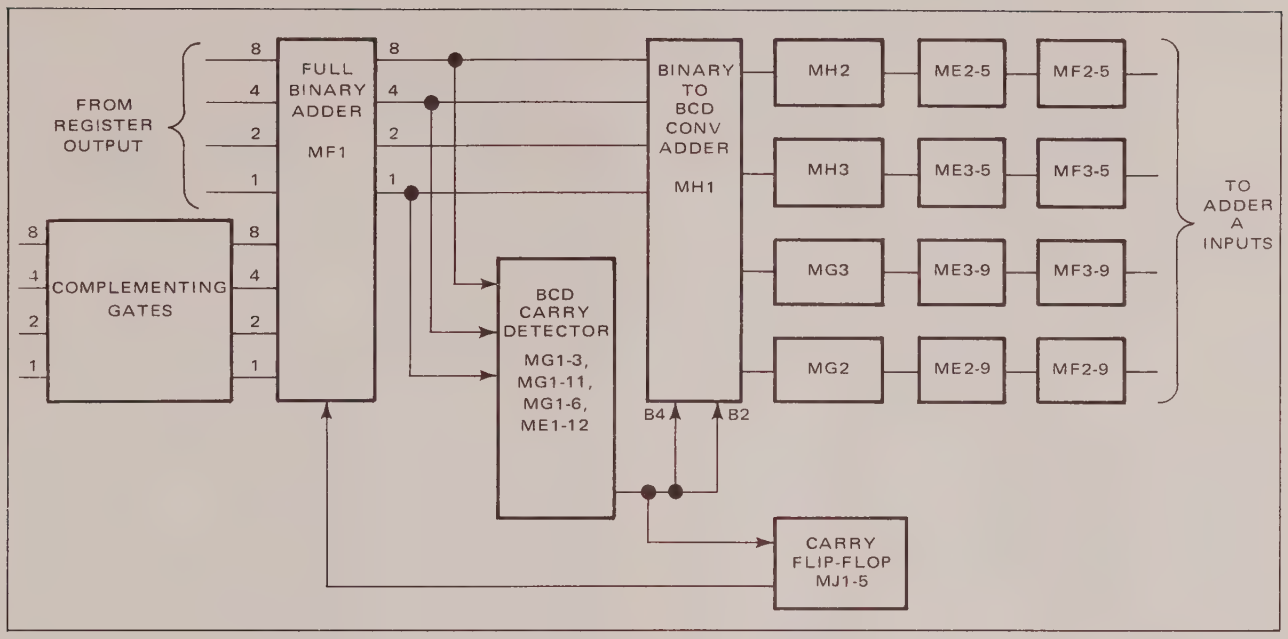


Figure 4.15 - Accumulator A, Block Diagram

the false-going transition of the most significant bit output of MJ5 clocks flip-flop MG5-9 to the set status.

4.109 With flip-flop MG5-9 in the set status, flip-flop MG5-5 is enabled to set. This is the output stage of the synchronizer whose output is added to the hundreds digit of the count circulating in the shift register at the end of bit period t3 of every word time. Thus, the status of this flip-flop cannot be updated during t3 time. It does, however, receive a CLOCK pulse at the end of every other bit period since the CLOCK signal is gated to the flip-flop clock input by the $\overline{t3}$ signal. The first CLOCK pulse received by flip-flop MG5-5 after flip-flop MG5-9 has been set clocks flip-flop MG5 to the set status. With MG5-5 set, MG5-6 is false. Thus, during the next t3 time, the output of NOR gate MH5-13 is placed at the true level in response to the false-going $\overline{t3}$ signal. The signal from MH5-13 is applied to the B1 input of the binary adder associated with register B. This causes a 1 to be added to the hundreds digit of the count circulating through the register. The signal from MH5-13 is also inverted by NOR gate MH5-1 and used to direct reset flip-flop MG5-9. With this flip-flop reset, flip-flop MG5-5 is enabled to reset in response to the next CLOCK pulse it receives. MG5-9 and MG5-5 then remain reset until the decade counter complete the next 100-count cycle.

4.110 Prior to the start of measurement time the two decade counters and the two synchronizer flip-flops are reset in response to the $\overline{\text{CLEAR}}$ signal from the sequence control logic. Counter MK5 is reset in response to a true signal from terminal 8 of flip-flop MA7 which is reset by the $\overline{\text{CLEAR}}$ signal. The first 10 MHz REF pulse gated to the clock line of counter MK5 does not increment the count because MK5 is held reset by flip-flop MA7-9. However, the trailing edge of this first pulse clocks flip-flop MA7-9 to the set status. This releases counter MK5 permitting subsequent 10 MHz REF pulses to be counted.

4.111 During a frequency measurement operation, the 10 MHz REF signal is gated to decade counter MK5 through NAND gate MM5-6 which is enabled by $\overline{\text{TI}}$ and $\Delta t_T 2$. $\overline{\text{TI}}$ from the mode control logic is continuously true during a frequency measurement operation. $\Delta t_T 2$ from the gate logic is true during the measurement time interval.

4.112 During a time interval measurement, the 10 MHz REF signal is gated to decade counter MK5 through NAND gate MM5-12 which is enabled by the ST (sample-time) signal from the time interval sequence control logic.

4.113 Accumulator A.

4.114 For the purpose of this discussion, accumulator A is defined to include register A, associated adders, a CARRY flip-flop, and conversion gates. See figure 4.15. Register A is identical to register B, described in paragraph 4.96. The other logic defined to be part of accumulator A is more complex than the comparable logic of accumulator B because accumulator A must be capable of performing the addition of two 10-digit numbers. Thus, while the largest output that can occur from the full adder in accumulator A is decimal 10, the full adder output in accumulator A can

Table 4.1 - Accumulator A Adder Outputs, Decimal Range of 10 to 19

Full Binary Adder MF1 Outputs					Decimal Equiv of Sum and Carry	Outputs From Binary to BCD Conversion Full Adder MH1					Decimal Equiv of Sum Only
Carry	Sum					Carry (Discarded)	Sum				
	8	4	2	1			8	4	2	1	
0	1	0	1	0	10	1	0	0	0	0	0
0	1	0	1	1	11	1	0	0	0	1	1
0	1	1	0	0	12	1	0	0	1	0	2
0	1	1	0	1	13	1	0	0	1	1	3
0	1	1	1	0	14	1	0	1	0	0	4
0	1	1	1	1	15	1	0	1	0	1	5
1	0	0	0	0	16	1	0	1	1	0	6
1	0	0	0	1	17	1	0	1	1	1	7
1	0	0	1	0	18	1	1	0	0	0	8
1	0	0	1	1	19	1	1	0	0	1	9

reach a maximum of 19. This occurs in the case where the two digits being added together are both 9's and there is a carry from the next lower order.

4.115 Because of the range of outputs possible from the full binary adder, the binary-to-BCD conversion logic must perform the following algorithm:

a. If the full adder sum and carry output is in the range of 0 through 9 (decimal), this output is passed to the register input without modification.

b. If the full adder sum and carry output is in the range of 10 through 19 (decimal), 6 (decimal) is added to the full adder sum output, the resultant carry is discarded, and the resultant sum is supplied to the register input. Also the CARRY flip-flop is set, to produce a carry into the next higher order.

4.116 The logic used to implement this algorithm includes gates used to detect the BCD carry range (that is, an output from the adder within the decimal range of 10 through 19) and a second full binary adder which is used to add 6 to the output of the first adder when required.

4.117 Adder MF1 is the main A-accumulator adder while adder MH1 serves as the binary-to-BCD conversion adder. The sum outputs of adder MF1 are applied to the A inputs of adder MH1. When the output of adder MF1 is in the range of 0 through 9, the B input to adder MF1 is zero. Thus, the sum outputs of adder MF1 pass unmodified to the inputs of the A-register. The 8, 4, 2, and carry outputs of adder MF1 are supplied to the gate configuration which supplies a true C_{OA} signal when the adder MF1 outputs are in the range of 10 through 19. The C_{OA} signal is supplied to the B2 and B4 inputs of adder MH1 as required to add 6 to the sum output of adder MF1 and is also applied to the data input of CARRY flip-flop MJ1-5. Thus, the CARRY flip-flop is clocked set whenever the output of adder MF1 is in the 10 to 19 range.

4.118 Table 4.1 shows the outputs from adders MF1 and MH1 for the decimal range of 10 through 19. The carry output of MF1 is used to place the C_{OA} signal at the true level for outputs in the decimal range of 16 through 19. The carry output of adder MH1 is not used.

4.119 Accumulator A Decade Counters and Synchronizer.

4.120 Because of the high frequency of the input signal (up to 50 MHz), special high-frequency a-c coupled J-K flip-flops are used to form the input decade counter. Figure 4.16 shows a simplified logic diagram of this counter.

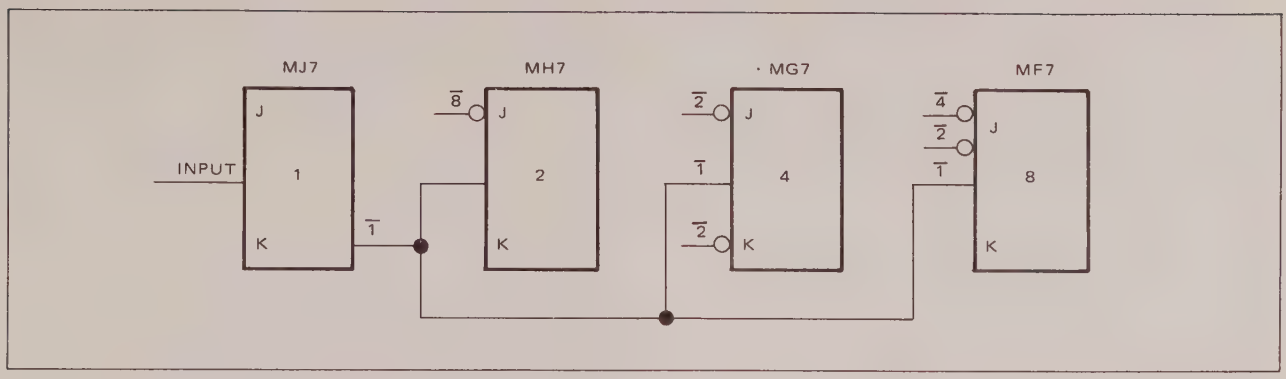


Figure 4.16 - High Speed Decade Counter Simplified Logic Diagram

The input (1) stage is toggled by each positive-going transition of the input signal. Positive-going transitions of $\overline{1}$ are used to clock the remaining stages. Where no inputs are shown to J or K gates, these gates are continuously enabled. The inputs shown must be low to enable clocking. The gating used provides a 1-2-4-8 BCD truth table. The counter operates exactly like a binary counter until the end of the 9-count (1001). At this time, the 8-stage is clocked reset and the 2-stage is inhibited from setting by the high level initially present on $\overline{8}$. Thus, the count recycles to 0000 rather than advancing to 1010 as it would in a binary counter. The outputs of the high-speed decade counter are applied to the TTL logic through transistor stages. At the start of a measurement time, the high-speed decade counter is reset by the CLEAR signal which controls its reset inputs via emitter follower Q8.

4.121 The 8 output of the high-speed decade counter is applied through transistor amplifier Q7 to the clock line of decade counter MH4. The output of this decade counter is applied to the clock line of divide-by-2 flip-flop MC4-5. The two decade counters and the divide-by-2 flip-flop operating in cascade form a scale-of-200 counter. As this counter recycles to zero following the count of 199, the true-going transition of the 0-output of flip-flop MC4-5 clocks flip-flop MC4-9 to the set status. This flip-flop together with flip-flop MC3-9 and the $\overline{\text{INCA}}$ gate form the synchronizer which is used to enter each carry from the scale-of-200 counter into the A-register. Since each carry is worth 200, it must be applied to the 2 input of the adder at t3 time (when the hundreds digit is applied to the adder). Flip-flop MC3-9 receives a clock pulse during every bit period except bit period t3. This insures that the status of MC3-9 does not change during the period when it must be applied to the adder. (The signal which clocks MC3-9 is received from NAND gate MD4-6, shown on sheet 1 of drawing 721081.) The first clock pulse received by flip-flop MC3-9 after flip-flop MC4-9 has set, clocks MC3-9 to the set status. With MC3-9 at the set status, the $\overline{\text{INC A}}$ line is placed at the false level during the next t3 time. With $\overline{\text{INC A}}$ false, the B2 input of the adder (MF1) is placed at the true level as required to add 2 into the hundreds order of the number circulating in the A-register. The $\overline{\text{INC A}}$ signal is also fed back from the adder input line through NOR gate ME5-13 to the direct reset input of flip-flop MC4-9 causing this flip-flop to reset. With flip-flop MC4-9 reset, the clock pulse applied to the clock line of MC3-9 during the next bit period resets MC3-9. The two synchronizer flip-flops then remain reset until the next carry is received from the scale-of-200 counter.

4.122 During DUMP time, the contents of the two decade counters are dumped into the units and tens orders of the number circulating in the A-register. This is accomplished by using the binary 1's of the decade counter outputs to preset the corresponding flip-flops of the two righthand stages of the A-register. This is identical to the dump into the B-register described in paragraph 4.100. In the case of the B-register, the contents of flip-flop MC4 of the scale-of-200 counter must also be dumped into the hundreds digit of the number circulating in the A-register. This is accomplished by gating the output of flip-flop MC4-5 to the preset input of the bit 1 flip-flop of the output stage of the A-register during bit period t3 when the hundreds digit resides in this stage. The dump can be handled by means of a preset because the hundreds digit is known to be even at this time. (All inputs during measurement time were 2's received from the synchronizer as previously described.)

4.123 The decade counters, the divide-by-2 flip-flop, and the synchronizer flip-flops are all reset at CLEAR time as required to initialize the logic.

4.124 B Inputs to A Accumulator Adder.

4.125 The A adder receives the following B inputs at various times during a frequency measurement sequence:

a. The $\overline{\text{INC A}}$ output of the synchronizer is applied to the B2 input of the adder at t3 time during the

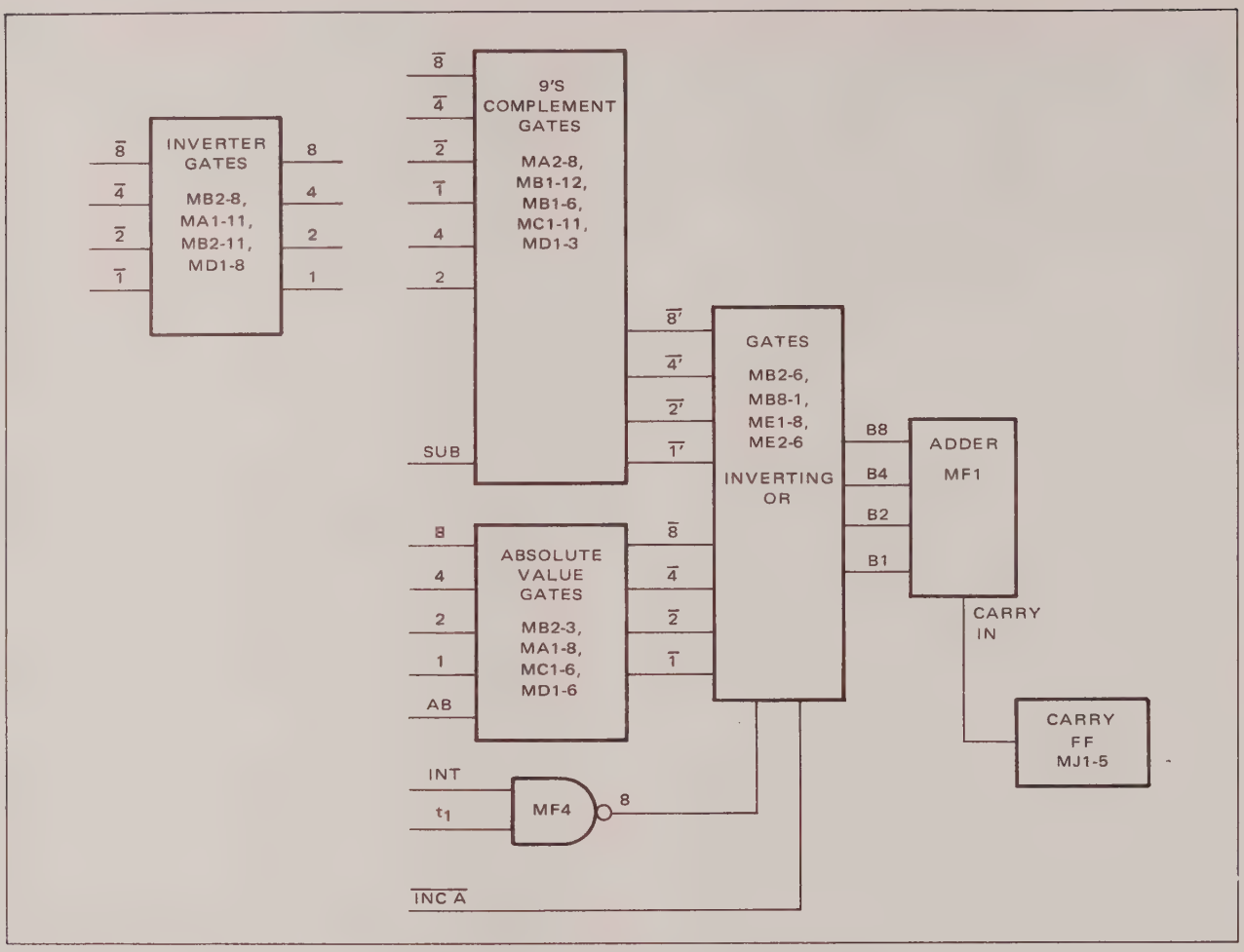


Figure 4.17 - Adder B Input Gates, Block Diagram

measurement time interval as explained in paragraph 4.121.

b. A 1 is applied to the B1 input of the adder during t1 time of the initiate (INT) word time. This is necessary in order to convert the 9's complement of the number from the B-register into the 10's complement during the first subtraction. (Subsequent 1's to convert 9's complements to 10's complements are obtained from the CARRY flip-flop as a result of end-around carry.)

c. The 9's complement of the data received from the B-register during each subtract word time is applied to the B inputs of the adder.

d. The absolute value of the data received from the B-register during each add-back (AB) word time is applied to the B inputs of the adder.

4.126 Figure 4.17 is a block diagram identifying the various gates associated with the adder B inputs. Complement data is received on the $\overline{8}$, $\overline{4}$, $\overline{2}$, $\overline{1}$ lines from the B-register when a divide routine is in progress. This is inverted to provide the absolute values required by the gates that are enabled during add-back. These gates are enabled by the AB signal from the sequence control logic. The gates which generate the 9's complement of each digit received from the B-register are enabled during subtract word times by the SUB signal from the sequence control logic. The 1 that is added during the initiate word time is supplied by gate MF4-8 in response to the coincidence of true t1 and INT levels. INT, from the sequence control logic is true during the initiate word time while t1 is true only during bit period t1. The $\overline{\text{INC A}}$ signal is gated in the synchronizer logic and passes to the B2 input of the adder through a gate in this logic which provides an inverting OR function.

4.127 The equations for conversion from absolute BCD to 9's complement BCD which are mechanized by the 9's complement gates are:

$$8' = \overline{8} \cdot \overline{4} \cdot \overline{2}$$
$$4' = \overline{4} \cdot 2 + 4 \cdot \overline{2}$$
$$2' = 2$$
$$1' = \overline{1}$$

where 8, 4, 2, 1 are the absolute BCD bits and 8', 4', 2', and 1' are the 9's complement bits.

4.128 Actually, the 9's complement gates supply the 1's complements of the 9's complement bits as indicated by the bars over the output signals in figure 4.17. However, these are inverted by the gates providing the inverting OR function.

4.129 Reset-Clear-Arm-Gate Logic.

4.130 A RESET signal occurs when the local RESET button is actuated, when a remote RESET signal is received, or when either an $\overline{\text{ABORT1}}$ or $\overline{\text{ABORT2}}$ signal occurs. $\overline{\text{ABORT1}}$ occurs when the time measurement count reaches 4 times the selected value before being terminated. This indicates either a loss of the unknown frequency input or a frequency which is too low to be measured using the selected measurement time interval. An $\overline{\text{ABORT2}}$ signal is received from the 500 MHz prescaler circuit board and indicates that the input signal being measured is out of the voltage range which allows accurate measurement. This signal can only occur when FREQ C is selected.

4.131 The RESET signal initializes the reset-clear-arm-gate logic by resetting the CLEAR synchronization flip-flop (MC2-5), the arm flip-flop (MC2-9), and the gate flip-flop (ML6-5). It also sets the CLEAR flip-flop (MC3-5). The RESET signal is inverted by NAND gate MA1-6 to provide the $\overline{\text{RESET}}$ signal which is supplied to the readout circuit board where it resets the display storage latch circuits causing zeros to be displayed in all digit positions of the display.

4.132 With the CLEAR flip-flop set all other control flip-flops in the high-speed switching logic are reset as required to initialize this logic. The flip-flops in the two righthand digit positions of the A and B registers are jammed in the reset status. Since the CLEAR signal is maintained for a minimum of one word time, this clears all 1's out of the A and B registers.

4.133 With the CLEAR flip-flop in the set status, CLEAR synchronizing flip-flop MC2-5 is enabled to set at the start of the next t10 bit period when it is clocked set by the true-going transition of the t10 pulse.

4.134 With MC2-5 set, the setting of arm flip-flop MC2-9 is enabled and this flip-flop is clocked set by the true-going transition of t10 occurring at the start of the next t10 time. The delay of one complete word period between the setting of MC2-5 and the setting of MC2-9 insures that the CLEAR signal has a minimum duration of one word period.

4.135 With arm flip-flop MC2-9 set, the CLEAR flip-flop is direct reset. At the same time, CLEAR synchronizing flip-flop MC2-5 is jammed in the set status. Thus, the data input of arm flip-flop MC2-9 remains true so that this flip-flop is not clocked to the reset status. With arm flip-flop MC2-9 in the set status, the data input of D-type gate flip-flop ML6-5 is enabled. With this flip-flop in the reset status, the output of NOR gate MK6-8 is held false. This enables the F_X signal to pass through NOR gate MK6-11 to the clock input of flip-flop ML6-5. If the FREQ A or FREQ C function is selected so that an unknown frequency is being supplied to the F_X line by the unknown frequency gates logic, then the first positive-going transition of this signal which occurs after the arm flip-flop has been set, clocks the gate flip-flop to the set status.

4.136 With the gate flip-flop in the set status, the $\Delta t_T 2$ signal becomes true while the $\overline{\Delta t_T 2}$ and $\overline{\Delta t_M}$ signals becomes false. During a frequency measurement operation, the $\Delta t_T 2$ signal is used to gate the 10 MHz REF signal to the decade counters associated with the B-register as required to accumulate a measurement time count. The false $\overline{\Delta t_M}$ level is used to gate the F_X signal to the decade counters associated with the A-register as required to accumulate a frequency count. Notice that the setting of the gate flip-flop which starts the measurement time is caused by the true-going transition of the unknown frequency signal.

4.137 During a frequency measurement operation, the arm flip-flop normally remains in the set status until the $\overline{\text{END}}$ signal is received from the end-abort logic. This indicates that the count being accumulated in the B-register has become equal to the selected measurement time interval. The false $\overline{\text{END}}$ level direct resets arm flip-flop MC2-9 via NAND gate MB4-11 and NOR gate MB3-13. With the arm flip-flop reset, the data input to the gate flip-flop is returned to the false level so that this flip-flop is reset by the next true-going transition appearing on its clock line. In the case of the frequency measurement operation, it is a transition of the F_X signal which clocks the gate flip-flop to the reset status. NOR gate MK6-11 continues to be enabled to pass F_X to the gate flip-flop clock line as a result of the true $\overline{\text{TI}}$ level being applied to one input of NOR gate MK6-8. The $\overline{\text{TI}}$ signal from the function selection logic is continuously true during a frequency measurement operation. The gate flip-flop is clocked both to the set status and to the reset status by positive-going transitions of the unknown frequency signal. Thus, the measurement interval is synchronized with

the unknown frequency and has a duration which is an integral number of cycles of the unknown frequency.

4.138 During a time interval measurement, the gate flip-flop is clocked set by the transition of the signal appearing on the F_X line as described for the frequency measurement case. In this case, this signal is the start pulse for the interval to be timed. With $\overline{TI}$ at the false level, the output of NOR gate MK6-8 becomes true when the gate flip-flop sets. This inhibits NOR gate MK6-11, isolating the F_X signal from the clock line of the gate flip-flop. At the same time, the arm flip-flop is direct reset via transistor Q1, NAND gate MB4-11, and NOR gate MB3-13. With the arm flip-flop reset, the next positive-going transition appearing on the clock line of the gate flip-flop clocks this flip-flop to the reset status. With NOR gate MK6-11 inhibited, the clock signal to reset the gate flip-flop must come from NOR gate MK6-3 which receives the TRIGGER B signal. This gate is enabled with transistor Q1 conducting. Thus, the first negative-going transition of TRIGGER B appears on the gate flip-flop clock line as a positive-going signal and resets the gate flip-flop. Thus, in the case of a time interval measurement, the measurement time is started by a transition of F_X and is ended by a transition of TRIGGER B. These two signals may actually be produced by the same input signal (if the SEP/COM switch is in the COM position) or may be produced by separate INPUT A and INPUT B signals respectively (if the SEP/COM switch is in the SEP position).

4.139 Dump Logic.

4.140 The dump logic includes three flip-flops; MA4-5, MA7-5, and DMP flip-flop MA4-9. The operation of this logic is the same for a time interval measurement sequence as for a frequency measurement sequence. The purpose of the three flip-flops is to provide a DMP signal which lasts for one word time and terminates at the start of bit period t1.

4.141 Flip-flop MA4-5 is clocked set by the true-going transition of the $\overline{\Delta t \top 2}$ which occurs at the time that the gate flip-flop is clocked to the reset status. This marks the end of the frequency measurement time or time interval measurement time. With flip-flop MA4-5 in the set status, the data input to D-type flip-flop MA7-5 is true. Thus, flip-flop MA7-5 is enabled to set in response to the next true-going transition of the t1 signal which is applied to its clock line. With flip-flop MA7-5 in the set status, the DMP flip-flop is similarly enabled to set in response to the next true-going transition of t1. As the DMP flip-flop sets, it resets flip-flops MA4-5 and MA7-5 via NOR gate MB5-1. With flip-flop MA7-5 in the reset status, the data input to the DMP flip-flop is false. Thus, the next true-going transition of t1 clocks the DMP flip-flop to the reset status.

4.142 The use of the DMP signal in transferring count data from the associated high-speed counters into shift registers A and B is described in the paragraphs covering the decade counters and synchronizers.

4.143 The $\overline{DMP}$ signal is supplied to the divide-routine sequence control logic and to the time interval sequence control logic where its false level enables a flip-flop in one of these logics to set at the time that the DMP flip-flop is reset. The particular sequence that is activated depends upon the status of the function selection logic.

4.144 Divide Routine Sequence Control Logic.

4.145 The divide routine is activated at the end of dump time when a frequency measurement is being performed. The activation of the divide routine starts with the setting of flip-flop MA5-9. This D-type flip-flop is enabled to set by the coincidence of false $\overline{DMP}$ and TI inputs to NOR gate MA6-13. The false $\overline{DMP}$ signal identifies the dump word time. The false TI signal from the function selection logic indicates that a frequency measurement sequence is in progress rather than a time interval measurement sequence. With its data input placed at the true level by NOR gate MA6-13, flip-flop MA5-9 is clocked set by the next positive-going transition of the t1 signal. At the same time, the DMP flip-flop is clocked reset. Thus, the output of MA6-13 is returned to the false level enabling flip-flop MA5-9 to reset in response to the next true-going transition of t1. As MA5-9 sets, it clocks the DIV and INT flip-flops to the set status. The DIV flip-flop remains in the set status for the remainder of the division routine. The INT flip-flop remains set for one word time during which various initializing operations are performed. INT is used to gate the t3 signal to the Z line. The Z signal is supplied to the readout circuit board where it is used to reset the units and quotients counters and to preset the digit counter. INT is supplied to the A-accumulator adder-B input gates where it is used to add a 1 to the contents of the A-register, in connection with generating the 10's complement of B for the first subtraction of the divide routine.

4.146 With the INT flip-flop in the set status, the data input of SUB flip-flop MD7-5 is held true via NAND gate MD5-6. This enables the SUB flip-flop to be clocked to the set status by the trailing edge of the CLOCK signal occurring during t10 time. (The clock signal for the SUB flip-flop, and also for the AB flip-flop which is discussed below, is obtained from NAND gate ME7-8 which receives the t10 and $\overline{CLOCK}$ signals.) As the SUB flip-flop sets, it direct resets the INT flip-flop via NOR gate MC5-4.

4.147 During each word time that the SUB flip-flop is in the set status, B is subtracted from A in the A-accumulator logic. If the subtraction leaves a positive or zero difference,

then the C_{OA} signal from the A-accumulator logic is true during bit period t10 of the word time. Under this condition, an INC Q pulse is supplied from NAND gate MD5-8. This pulse increments the quotient counter on the readout board.

4.148 With the SUB flip-flop in the set status and with C_{OA} true, the data input of the SUB flip-flop is held true by NAND gate MD6-11 via NAND gate MD5-2. Under this condition, the clock pulse applied to the SUB flip-flop during t10 time does not affect its status and the SUB flip-flop remains set for another word period. When a subtraction yields a negative difference, then C_{OA} is false during t10 time. Under this condition, the data input of the SUB flip-flop is false and the SUB flip-flop is clocked reset at the end of t10 time. At the same time, with $\overline{SUB}$ and C_{OA} both false, the data input of the AB flip-flop is held true by NOR gate MC5-13. Thus, the AB flip-flop is clocked to the set status as the SUB flip-flop is clocked to the reset status.

4.149 With $\overline{SUB}$ true, the data input of the AB flip-flop is false. Thus, the AB flip-flop remains set for only a single word time. Also, with $\overline{AB}$ false, the data input of the SUB flip-flop is again placed at the true level. Thus, when AB resets, SUB again sets. During each word period when the AB flip-flop is in the set status, the subtraction which produced the negative balance is cancelled by adding the contents of B to A. Also, the contents of A is shifted one character position to the left (by inhibiting the clocking of the A-register during bit period t10).

4.150 The false $\overline{AB}$ level is supplied to the readout board where it enables the transfer of the quotient accumulated in the quotient counter into the display latch currently being pointed to by the digit counter. During bit period t9 of each AB word time, the H pulse is gated to the F line. The F pulse is supplied to the readout board where it is used to reset the quotient counter in preparation for the accumulation of the next quotient digit. Also, the F pulse is gated either to the INC U line or to the INC D line depending upon the status of flip-flop MD7-9. This flip-flop is in the reset status at the start of the routine. It is clocked set by the first INC Q pulse of the routine.

4.151 If the frequency count accumulated in the A accumulator during measurement time is smaller than the measurement time count accumulated in the B-register, then the contents of the A accumulator must be shifted left one or more times before a positive or zero difference can be obtained during subtraction. This means one or more passes through add-back before the MD7-9 flip-flop is set. During each such pass, the INC U pulse increments the units counter on the readout board. Each time that the units count is incremented, the significance of the display digit positions is decreased by a factor of 10 either by shifting the decimal point one position to the left or by changing the units indication by a factor of 1000 and moving the decimal point two places to the right. During each such pass through add-back, the zero contents of the quotient counter is transferred into the display latch circuit associated with the left display digit. This is the digit position which is pointed to by the preset count in the digit counter and the digit counter is not incremented until the add-back which occurs after a positive or zero difference has been obtained.

4.152 When the first positive or zero difference is obtained, an INC Q pulse occurs, for the first time producing a non-zero quotient count. At the same time, this first INC Q pulse sets the MD7-9 flip-flop so that subsequent F pulses are gated to the INC D line rather than to the INC U line. The subtractions continue until a negative difference is again obtained. During the add-back word time that results, the first non-zero quotient is transferred from the quotient counter into the display latch associated with the left display digit. Following this, the F pulse occurring during t9 time is gated to the INC D line so that the digit count is incremented as required to point to the next digit position to the right. For the remainder of the routine, the digit count is incremented during each pass through add-back as required to transfer each successive digit (whether zero or non-zero) into the display digit position to the right of that occupied by the preceding digit.

4.153 The maximum units count is limited to 8. If 8 passes through add-back occur without a positive or zero difference being obtained, then on the 8th pass, the INC U pulse increments the units count to 8. This causes the D ENABLE signal from the readout board to go false. This is inverted to a positive transition by NAND gate MB7-6 as required to clock flip-flop MD7-9 to the set status. If the next subtraction also yields a negative difference, then the digit count is incremented before the most significant non-zero digit of the quotient has been obtained. Thus, in this case, the left digit of the final display is a zero.

4.154 Once flip-flop MD7-9 is set, so that the digit count is incremented during each pass through add-back, the duration of the routine is limited to 10 additional passes through add-back. The INC D pulse on the 10th such pass increments the digit count to 10. This causes the EXIT signal from the digit counter to go false. With EXIT at the false level, the direct reset inputs of the DIV, SUB, and AB flip-flops are all placed at the false level via NAND gates MD6-3 and MD6-8. Thus, the division routine is terminated.

4.155 With EXIT false, the data input of flip-flop MC7-5 is placed at the true level via NAND gate MB7-11. If the unit is in the AUTO status, the next true-going transition of t1 clocks flip-flop MC7-5 to the set status. When MC5-7

sets, it direct sets the CLEAR flip-flop via NOR gate MB3-10. As the CLEAR flip-flop sets it direct resets flip-flop MC7-5 via NOR gate MB5-13. The setting of the CLEAR flip-flop initiates another frequency measurement sequence (assuming that the function selection has not been changed).

4.156 If the unit is in the HOLD status, flip-flop MC7 is jammed in the reset status in response to the true HOLD level being applied to NOR gate MB5-13. Thus, in this case, another measurement cycle is not initiated until a reset occurs.

4.157 Time Interval Sequence Control Logic.

4.158 When the time-interval measurement function is selected, then the $\overline{TI}$ signal from the function selection logic is at the false level. Under this condition, the false $\overline{DMP}$ signal occurring during the dump word time places the data input of the TI TRNF flip-flop (MA5-5) at the true level via NOR gate MA6-1. This flip-flop is then clocked set by the same t1 transition which resets the DMP flip-flop. With $\overline{DMP}$ returned to the true level, the data input of the TI TRNF flip-flop becomes false. Thus, the TI TRNF flip-flop remains set for one word time. During this word time the false $\overline{TI\ TRNF}$ signal is supplied to the display logic where it is used to enable the transfer of the time interval count from the A-register into the display latch circuits.

4.159 When the TI TRNF flip-flop resets, it clocks the ST flip-flop to the set status. With ST true, the B-accumulator is enabled to accumulate a count of 10 MHz REF pulses. When this count reaches the selected measurement time value, then a false $\overline{END}$ signal is received from the end-abort logic. This direct resets the ST flip-flop via NOR gates MA6-4 and MA6-10.

4.160 As the ST flip-flop resets, it clocks flip-flop MB6-9 to the set status. This places the data input to flip-flop MC7-5 at the true level. If the unit is in the AUTO status, flip-flop MC7-5 is clocked set by the next t1 pulse. This causes the CLEAR flip-flop to set as required to start another measurement sequence. When the CLEAR flip-flop sets, it direct resets the MC7-5 flip-flop. If the unit is in the HOLD status, then flip-flop MC7-5 is held reset by the true HOLD level applied to NOR gate MB5-13 and another measurement sequence is not initiated until a reset pulse occurs.

4.161 Time Base Gates.

4.162 The time base signal (TB) is used by the end-abort logic to determine the particular digit of the reference count that is monitored to determine when the measurement time has been completed. The appropriate digit for monitoring depends upon the measurement time selection. For example, a measurement time of 0.1 second is represented by a count of 1,000,000 in the B-accumulator. Therefore, for this measurement time selection, the 10^6 digit of the count must be monitored. Since this digit is available at the output of the B-accumulator at t7 time, the .1 measurement time signal is used to gate the t7 signal to the TB line. Similarly, for each other possible measurement time selection, the appropriate tx signal is gated to the TB line.

4.163 Measurement Time Selection Gates.

4.164 The measurement time selection signals from the selection logic are supplied to four NOR gates (MM4-1, MM4-13, MM4-10, and MM4-4) which are enabled by the false level on the $\overline{TI}$ line when a frequency measurement function is selected. The measurement time selection outputs of these gates are supplied to the readout board where they are used by the digit blanking logic. Since these signals are supplied only when a frequency measurement function is selected, digit blanking is disabled during time interval measurements.

4.165 Mode, Measurement Time, and Function Switches.

4.166 Switches S2 through S13 provide the local means for controlling mode, measurement time, and function. For models not provided with remote programming, the switches provide the only means of control. For these models, the outputs of the selection switches are jumpered directly to the adjacent selection lines. For example, pin 22 is jumpered to pin Z of J4 so that the output from TI switch S12 is connected to the TI line. For models which can accept remote programming, the connections between the switch outputs and the various selection lines are completed in the program signal conditioning logic when the REMOTE function is not selected. When the REMOTE function is selected, the status of the various selection lines is controlled in accordance with the status of the remote programming inputs and the local switch settings are not effective.

4.167 Single-Channel 50 MHz Preamplifier.

4.168 This circuit consists of the following sections:

a. The input network which provides AC or DC input coupling and an appropriate level of attenuation in accordance with the positions of the AC and RANGE switches.

b. A FET buffer amplifier which isolates the input network from the remainder of the circuit.

c. A differential trigger amplifier which converts the input signal into the square waveform required for counting.

d. Output gating which selects the phase of the output so as to provide triggering on the positive-going or negative-going slope of the input waveform, as determined by the position of the Plus Slope Switch (or by the RANGE switch when placed in the PRESET position).

4.169 Input A is applied from the front panel connector to the AC switch. When this switch is in the AC position, the input is coupled through capacitor C1. When the switch is in the DC position, capacitor C1 is bypassed and the input is coupled to the gate circuit of the FET buffer amplifier through a resistive path, unless the RANGE switch is in the PRESET position. In this latter case, the input is coupled to the gate circuit of Q1 through capacitor C4.

4.170 Attenuation of the input signal is provided by a voltage divider which employs resistors R2 through R6 and capacitors C2, C3, and C5 through C8. When the RANGE switch is in the .1 position, the input signal is picked off the top of the divider and is not attenuated. Pickoff points for the 1, 10, and 100 positions of the switch provide attenuations of 1/10-th, 1/100-th, and 1/1000-th respectively. The 1/10-th pick-off point is also used as the pick-off point for the PRESET position. However, when PRESET is selected, the signal from the 1/10-th pick-off point is coupled to the FET buffer through capacitor C4.

4.171 If the RANGE switch is positioned in accordance with the amplitude of the signal being applied to the input A connector, then a signal on the order of 100 millivolts or less is supplied to the FET buffer. Diode limiting is provided by diodes CR1 through CR4 in order to protect the FET buffer from being overdriven. The diodes are connected so that the signal at the junction of resistors R8 and R9 is limited to within $\pm$ two diode drops of ground.

4.172 FET Q1 functions in connection with amplifier Q2 as a bootstrapped source follower. Bootstrapping is obtained by applying the signal developed at the drain electrode of Q1 to the base of Q2. A portion of the output of Q2 is then fed back to the source electrode of Q1 where it appears in phase with the signal applied to the gate electrode of Q1. In this way, the voltage difference between the gate and source electrodes of Q1 is maintained at an approximately constant level.

4.173 Potentiometer R14 in the source circuit of Q1 provides one component of the input signal to the differential trigger amplifier. This signal is supplied through inductor L1 to the base of Q3. Because of the inductance in this path, the gain provided by this path drops off with increasing frequency. However, a second signal component is obtained through a high-pass path from the collector of Q2. Notice that since only a portion of the signal developed at the collector of Q2 is fed back to the source electrode of Q1, the gain of Q2 is permitted to exceed unity. The gain of Q2 is determined by the value of factory-selected R13. This provides a means of equalizing the response of the circuit over the required frequency range. The setting of potentiometer R14 adjusts the bias of the base circuit of Q3 and this, in turn, determines the switching threshold under PRESET conditions. (The switching threshold is varied by means of LEVEL adjustment potentiometer R33 for other positions of the RANGE switch.)

4.174 The differential trigger amplifier employs two differential amplifier stages and two emitter followers which provide positive feedback for the second differential amplifier stage. The input differential amplifier stage employs transistor Q1 and Q8. The switching threshold of this circuit is determined by the reference potential applied to the base of Q8. When the RANGE switch is at the PRESET position, the switching threshold for this circuit is 0 volts. When the RANGE switch is in any other position, the switching threshold can be adjusted to be positive or negative by adjusting the position of LEVEL potentiometer R33.

4.175 The second differential amplifier stage employs transistors Q5 and Q6. Emitter followers Q7 and Q4, driven by the outputs from Q5 and Q6 respectively provide positive feedback which produces regenerative switching action similar to that in a flip-flop. However, the positive feedback is limited by the introduction of negative feedback through resistor R25. The feedback parameters have been adjusted so as to produce an amount of hysteresis which optimizes the noise immunity of the circuit. To understand the hysteresis effect, consider that when Q5 is conducting and Q6 is cut off, the emitter of Q3 is positive with respect to the emitter of Q7. Since Q3 is the source of forward bias for Q5, and Q7 is the source of forward bias for Q6, this difference in potential must be overcome by the differential signal between the base of Q4 and the base of Q8 before Q5 can be cut off and Q6 can be turned on. With Q5 cut off and Q6 conducting, the situation is reversed. The emitter of Q7 is now positive with respect to the emitter of Q3. This reversed difference must, of course be overcome by a reverse differential signal between the base circuits of Q4 and Q8 in order to switch the circuit in the opposite direction.

4.176 The effect of the difference in potential between the emitters of Q3 and Q8 on the base circuits of Q5 and Q6 is decreased by the presence of resistor R25. This resistor has been selected to set the hysteresis at the required

level. Specifically, hysteresis is on the order of 15 millivolts when referred to the base circuits of Q4 and Q8.

4.177 The output of the differential trigger amplifier is taken from the emitter of emitter follower Q7. This signal is applied to an input of NOR gate M1-8 and also to an input of NOR gate M1-6. When the Plus Slope switch (+) is in the plus (+) position or when the RANGE switch is in the PRESET position, NOR gates M1-8 and M1-3 are enabled by low levels applied to their control inputs via the controlling switch. Under this condition, the signal from the emitter of Q7 passes through NOR gates M1-8 and M1-3 and appears uninverted on the TRIGGER A line. Since the signal at the emitter of Q7 is in phase with respect to the signal at the INPUT A connector, this means that the TRIGGER A signal is in phase with the INPUT A signal. When the RANGE switch is not in the PRESET position and the Plus Slope switch is not in the plus (+) position, then the control inputs of NOR gates M1-8 and M1-3 are pulled high through resistor R35 and this output path is disabled. At the same time, the high signal from resistor R35 places the output of NOR gate M1-11 at the low level. This signal enables NOR gate M1-6 to pass the output signal from the emitter of Q7. Since the output signal now passes through only a single NOR gate between the emitter of Q7 and the TRIGGER A line, it is now inverted with respect to the INPUT A signal. It is the positive-going transition of the TRIGGER A signal which is used as an internal triggering signal. Thus, when TRIGGER A is in phase with INPUT A, the unit triggers on the positive slope of the INPUT A signal and when TRIGGER A is out of phase with INPUT A, the unit triggers on the negative slope of the INPUT A signal.

4.178 Dual 50 MHz Preamplifier.

4.179 This circuit board provides two preamplifier channels which are essentially the same as the single channel provided by the single-channel 50 MHz preamplifier circuit board. Channel A of the dual preamplifier obtains its input signal from the INPUT A connector. Channel B obtains its signal from the SEP switch. When this switch is in the SEP position, the INPUT B connector is connected to the input of channel B. In this mode, the counter is used to measure an interval whose start is defined by a signal on the line connected to INPUT A and whose termination is defined by a signal on the line connected to INPUT B. When the SEP switch is placed in the COM position, channel B, like channel A, receives its input from the INPUT A connector. Thus, in this case, both channels receive the same input signal. This allows the timing of intervals between pulses appearing on the same signal line.

4.180 The TRIGGER A signal is applied to the base circuit of transistor Q9 whose output is coupled to the MARKER A line. The RC circuit at the base of Q9 has a time constant of 1 μsec so that a short MARKER A pulse is obtained in response to each transition of the TRIGGER A signal. The MARKER A pulse is supplied to external equipment for use in defining the start of a time interval for the purpose of intensifying a scope display for the duration of that interval.

4.181 Channel B is identical to channel A except that the gates for selecting the phase of the TRIGGER B signal are configured differently and the input circuit of the MARKER B stage differs somewhat from the MARKER A stage. In the case of channel B, the in-phase output signal from emitter follower Q107 is applied to the TRIGGER B line through NOR gate M101-6 when the RANGE switch is in the PRESET position or when the Plus Slope switch is in the Plus (+) position. Thus, in this case, these switch positions provide a TRIGGER B pulse which is out of phase with the input signal being received from the SEP switch. However, in the case of the TRIGGER B signal, it is the negative-going transition which is used internally. Thus, when PRESET or Plus is selected, it is still the positive slope of the input signal which causes the triggering to occur.

4.182 When the RANGE switch is not in the PRESET position and the Plus Slope switch is not in the Plus position, then the out-of-phase output from the emitter of Q103 is applied to the TRIGGER B line through NOR gate M101-3. Thus, in this case, the TRIGGER B signal is in phase with the input signal and triggering occurs on the negative-going slope of the input signal.

4.183 The MARKER B amplifier receives the inverse of the TRIGGER B signal from NOR gate M101-8 which is continuously enabled. Thus, the positive-going MARKER B pulse occurs in response to the positive-going transitions of TRIGGER B.

4.184 500 MHz Prescaler.

4.185 This circuit consists of the following sections: (See figure 4.18).

a. A constant-impedance diode attenuator used to maintain automatic gain control over a 55 dB range of input signal levels.

b. A high pass filter.

c. A four-stage wideband amplifier (Q1 through Q4).

d. A diode detector (CR10) used to detect the level of the wideband amplifier output for use in the AGC amplifier.

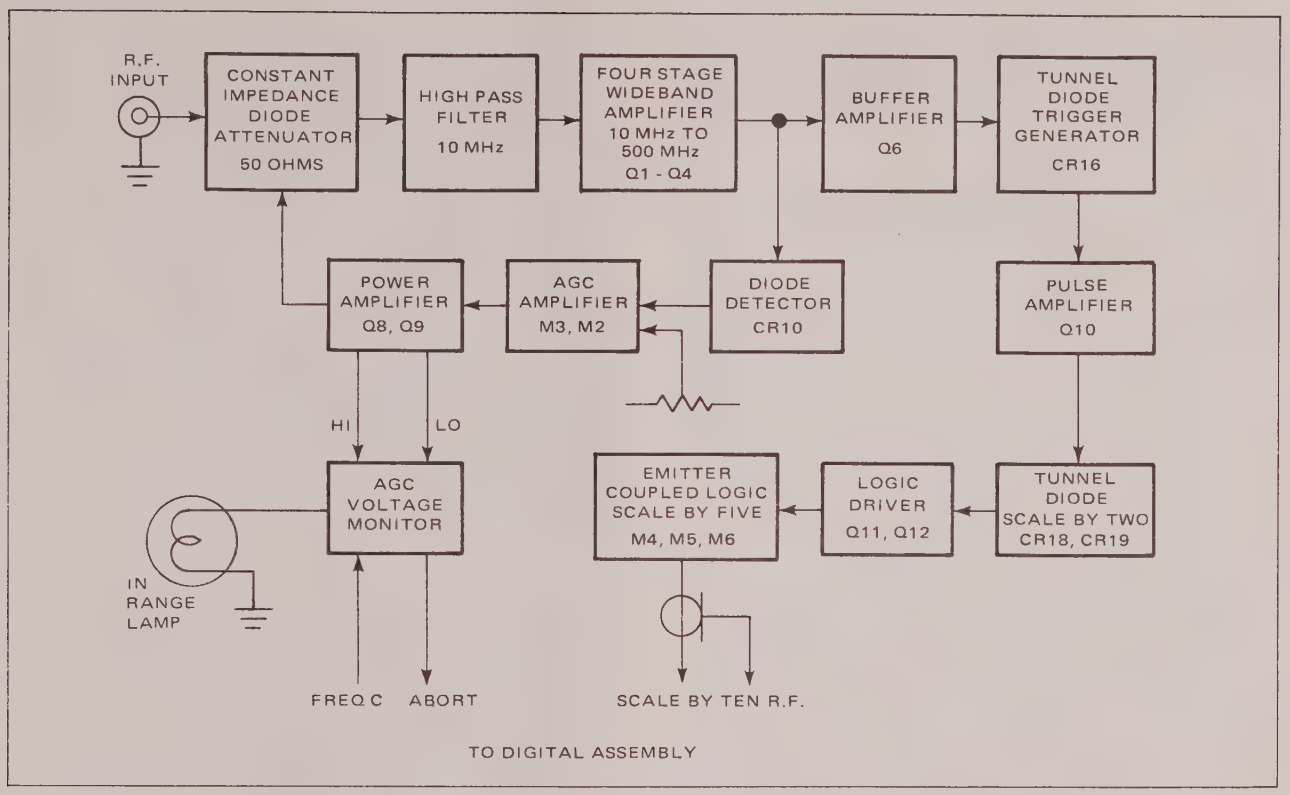

R.F. INPUT
CONSTANT IMPEDANCE DIODE ATTENUATOR 50 OHMS
HIGH PASS FILTER 10 MHz
FOUR STAGE WIDEBAND AMPLIFIER 10 MHz TO 500 MHz Q1 - Q4
BUFFER AMPLIFIER Q6
TUNNEL DIODE TRIGGER GENERATOR CR16
POWER AMPLIFIER Q8, Q9
AGC AMPLIFIER M3, M2
DIODE DETECTOR CR10
PULSE AMPLIFIER Q10
HI
LO
AGC VOLTAGE MONITOR
EMITTER COUPLED LOGIC SCALE BY FIVE M4, M5, M6
LOGIC DRIVER Q11, Q12
TUNNEL DIODE SCALE BY TWO CR18, CR19
IN RANGE LAMP
FREQ C
ABORT
SCALE BY TEN R.F.
TO DIGITAL ASSEMBLY

Figure 4.18 - 500 MHz Prescaler, Block Diagram

e. An AGC amplifier (M3, M2) which introduces the necessary gain in the AGC loop.

f. A power amplifier (Q8, Q9) which accepts the output of the AGC amplifier and drives the constant impedance diode attenuator network.

g. An AGC voltage monitoring circuit (enabled only when the FREQ C function is selected) which turns on the IN RANGE lamp when the AGC voltage level indicates that the input signal is in range and supplies an ABORT signal when the AGC voltage level indicates that the input signal is out of range.

h. A buffer amplifier (Q6), tunnel diode pulse generator (CR16), and pulse amplifier (Q10) which provide pulses required for counting.

i. A tunnel diode binary (CR18 and CR19), a logic drive amplifier (Q11, Q12), and a three-stage flip-flop scale-of-5 ring counter (M4, M5, M6) which together divide the pulse rate by a factor of 10.

4.186 The diode attenuator includes diodes CR4 and CR6 which are in series with the input signal and diodes CR1, CR5, and CR8 which are in shunt with the input signal. Under zero input conditions, CR4 and CR6 receive sufficient forward bias so that they appear as an extremely low series impedance while the shunt diodes are reverse biased and appear as very high impedances. As the input signal increases, the bias signal is modified so that the impedance of the series diodes increases and the impedance of the shunt diodes decreases. Zener diodes CR2 and CR3 are used to develop a positive fixed bias signal which is applied to the cathodes of the two series diodes and to the anodes of shunt diodes CR6 and CR1. The AGC output from the power amplifier is applied to the diode attenuator network through diode CR7. While this signal is sufficiently positive with respect to the fixed bias signal from the zener diodes, it forward biases the series diodes of the attenuator and reverse biases the shunt diodes.

4.187 As the level of the input signal increases, the AGC output becomes less positive. This reduces the forward bias on the series diodes and the reverse bias on the shunt diodes causing an increase in attenuation. As the input level continues to increase, the series diodes become reverse biased and the shunt diodes become forward biased. Within the dynamic range of the loop, the output of the diode attenuator is maintained at a relatively constant level.

4.188 The output of the diode attenuator is applied to a high-pass filter employing capacitor C15 and a 2.2 UH shunt inductor. This filter discriminates against frequencies below 10 MHz so as to avoid overloading the amplifier in response to low frequency signals.

4.189 The output of the high-pass filter is applied to the first stage of the four-stage wideband amplifier. The four stages of this amplifier are essentially the same. Consider stage Q2. Negative feedback is provided from the collector of Q1 to the base of Q1 through a frequency sensitive network which provides an inverse relationship between feedback and frequency. This provides the greatest feedback at the low end of the band where the transistor gain is highest and the minimum feedback at the high end of the band where the transistor gain is lowest. In this way, stage gain is maintained relatively constant over the entire band.

4.190 The output from amplifier stage Q4 is applied to the input circuit of buffer amplifier Q6 and is also applied to the diode detector circuit which employs CR9 and CR10. CR9 functions as a d-c restorer which clamps positive-going excursions of the input waveform to ground. CR10 functions in conjunction with capacitor C36 as a negative peak detector. Excursions of the input signal which are negative with respect to the voltage across capacitor C36 produce forward bias across CR10 and resultant charging current through C36. Thus, C36 tends to charge to the peak voltage of the input signal.

4.191 The diode detector output is summed with a reference signal from potentiometer R61 at the inverting input of differential amplifier M3. The amplifier functions to integrate the algebraic sum of the diode detector output and the reference voltage. Because of the integration, the detector output can be maintained exactly equal to the reference voltage under steady-state conditions. (Under this condition, there is zero difference voltage at the amplifier input. In response to this condition, the amplifier maintains a constant output as required to maintain the attenuation at the current level.) Potentiometer R64 provides the means for setting the loop output at the desired level.

4.192 The output of amplifier M3 is applied to amplifier M2. This amplifier functions as an inverter with a non-linear gain characteristic. This non-linear gain characteristic is introduced by the presence of diode CR15 in the feedback network. The non-linear characteristic of the diode causes the feedback ratio to change as a function of voltage and this, in turn, causes the gain of the amplifier to be a function of the input voltage level. This non-linear characteristic compensates for the non-linear characteristic of the diode attenuator network.

4.193 The output of amplifier M2 is applied to the base circuits of emitter followers Q8 and Q9 which provide the drive required to control the diode attenuator network. It is also applied to a monitor circuit which controls the $\overline{\text{ABORT}}$ line and the IN RANGE lamp. A simplified diagram of this circuit is shown in figure 4.19. The output gates of this circuit which control the $\overline{\text{ABORT}}$ line and the IN RANGE lamp are enabled only when the FREQ C signal from the function selection logic is true. This indicates that the prescaler is in use. Under this condition, the circuit outputs are controlled in accordance with the status of the trigger circuit which employs gates M1-3 and M1-11. When the input signal level is within the range which insures accurate measurement, then the output of M1-11 is low. This places the $\overline{\text{ABORT}}$ line at the true (inactive) level. With $\overline{\text{ABORT}}$ and FREQ C both true, the output of M1-6 is driven low. This places +5 volts across the IN RANGE lamp causing it to light and indicate that the signal is within range.

4.194 As the input signal level becomes smaller, the power amplifier output becomes more positive. This drives the collector of Q7 more positive. When the input signal level decreases to a level at which accurate measurement is no longer insured, the signal at the collector of Q7 becomes sufficiently positive to place the output of M1-3 at the false level. This, in turn, switches the output of M1-11 to the true level placing the $\overline{\text{ABORT}}$ line at the active level and turning off the IN RANGE lamp. Notice that with the output of M1-11 at the true level, the input level at M1-1 is raised further due to the feedback through resistor R43. This provides the hysteresis necessary to prevent the circuit from oscillating between its two states under the condition when the AGC voltage is just at the switching threshold level.

4.195 As the input signal level increases, the power amplifier output becomes less positive. When the input signal reaches an excessive level, the input of gate M1-11 is pulled low through resistor R42 and diode CR11. This, again switches M1-11 to the high level placing the $\overline{\text{ABORT}}$ line at the low (active) level and turning off the IN RANGE lamp. The $\overline{\text{ABORT}}$ signal is fed back to the input of M1-11 through resistor R41 as required to produce hysteresis in this branch of the trigger circuit.

4.196 Returning from the AGC circuit to the main signal path, the output of amplifier Q4 is applied to buffer amplifier Q6 as previously noted. This amplifier provides one stage of amplification that is outside the AGC loop. The output of this amplifier is applied to tunnel diode trigger generator CR16. The triggering point of this circuit is set by means of potentiometer R71. The output of the trigger generator is applied to pulse amplifier Q10. This amplifier

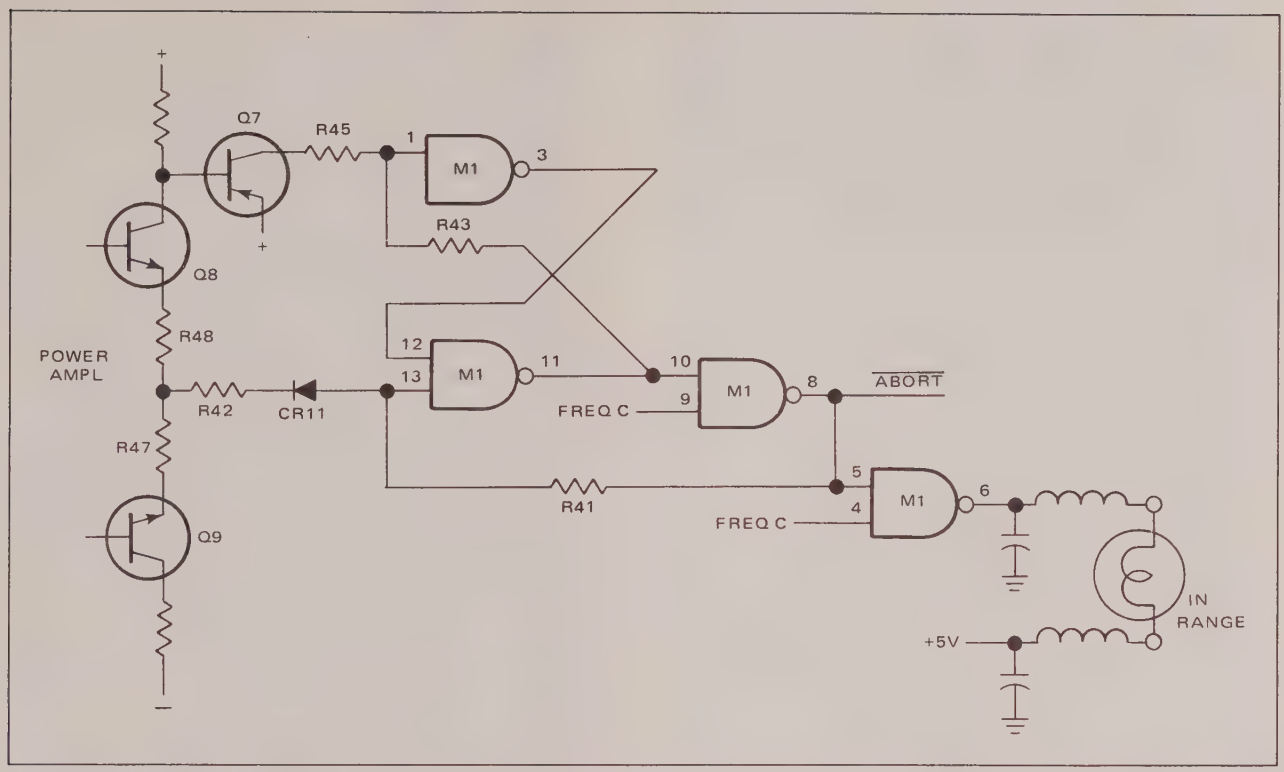


Figure 4.19 - AGC Voltage Monitoring Circuit, Simplified Schematic Diagram

contains delay lines in both the emitter and collector circuits. Reflections from these delay lines re-enforce and sharpen the pulse. The output of the pulse amplifier is applied to a tunnel diode binary employing tunnel diodes CR18 and CR19. When its bias has been properly adjusted by means of potentiometer R79, this circuit reverses state in response to each input pulse as required to divide the input frequency by 2.

4.197 The output from the tunnel diode binary is supplied via amplifier Q12 and emitter follower Q11 to the clock line of a scale-of-5 ring counter employing high-speed flip-flops M4 through M6. These D-type flip-flops are connected so that M4 sets only when M5 and M6 are both reset, M5 sets only when M4 is set, and M6 sets only when M5 is set. The resulting count cycle is 000, 100, 110, 011, 001, 000, etc. This provides an output from M4-3 which is one-tenth of the input frequency. This signal is supplied to the high-speed switching logic board on the TRIGGER C line.

4.198 Single Program Signal Conditioner.

4.199 This circuit board provides a single 50 MHz preamplifier channel with provisions for both local and remote control of its range, triggering level, and coupling parameters. The circuit board is also provided with logic which permits either local or remote programming control of mode, measurement time, and function selections.

4.200 Sheet 1 of the referenced drawing illustrates the mode, measurement time, and function selection control. The control mode is determined by the status of the alternate-action REMOTE switch on the high-speed switching circuit board. If this switch is in the local control status, then the $\overline{\text{RMT}}$ signal from the high-speed switching circuit board is true. This enables eight NAND gates through which the mode, function, and measurement time selection signal inputs from the high-speed switching circuit board are applied to the corresponding output lines to that circuit board. The mode selection input signals are HOLD and RESET. The measurement time selection inputs are .001, .01, .1, and 1. (The 10 second measurement time is selected by default if none of the other time selection signals is true.) The function selection inputs are FREQ A and FREQ C.

4.201 When the REMOTE switch on the high-speed switching circuit board is in the REMOTE control status, then the RMT signal from the high-speed switch board is

true and the $\overline{RMT}$ signal is false. Under this condition, the output selection lines are controlled in accordance with the status of the remote input signals. The J and K inputs are applied to decoder M1 which controls the function output lines. This decoder is enabled by the false level on the $\overline{RMT}$ line. If the J and K inputs are both false, the FREQ A output line (J14-C) is placed at the true level. If K is true and J is false, the FREQ C output line (J14-H) is placed at the true level.

4.202 The measurement time selection output lines are controlled in the remote control mode by a second section of decoder module M1. The selection code inputs to this decoder section are provided on the R, S, and T lines. The R signal is inverted and applied to a NAND gate which controls the $\overline{EN}$ input of the section. This NAND gate also receives the RMT signal. Thus, the $\overline{EN}$ line is placed at the false (enabling) level only if RMT is true and R is false. A true R input represents the 10 second measurement time selection. In this case, all of the measurement time selection outputs from this logic are false. If R is false, then one of the measurement time selection outputs is true in accordance with the status of the T and S input signals as follows:

R	S	T	Selected Output	Pin (J14-)
0	0	0	.001	4
0	0	1	.01	5
0	1	0	.1	14
0	1	1	1	15

4.203 In the remote control mode, two gates which receive the remote RESET and HOLD signals are enabled by the true RMT level. Thus, these two signals control the output RESET and HOLD selection lines.

4.204 The 50 MHz preamplifier channel and its associated range, triggering level, and coupling conditioning logic are illustrated on sheet 2 of the referenced drawing. The basic preamplifier consisting of the FET buffer and the differential trigger amplifier is identical to the corresponding preamplifiers used in non-programming units and described in paragraph 4.167. The input attenuator network is designed differently in order to facilitate programmed control of range selection. The output phase selection is accomplished by selecting either of two out-of-phase signals from the basic preamplifier rather than by selecting either one or two inversions of the single preamplifier output as in the case of the non-programmable unit.

4.205 As in the case of the mode, time measurement, and function selection logic, local or remote control of preamplifier conditioning is selected in accordance with whether the $\overline{RMT}$ or RMT signal from the high speed switching circuit board is at the true level.

4.206 When the local control mode is selected, the false RMT level enables deck A of RANGE switch S3. This deck controls the status of the input attenuator network.

4.207 Control of the attenuation network in either the local or the remote control mode is exercised via transistors Q108, Q109, and Q110. Each of these transistors controls the ground return for an associated shunt resistor and an associated shunt capacitor in the input attenuator network. The ground return for the shunt resistor is completed via a FET switch which is turned on when the associated drive transistor conducts. The ground return for the shunt capacitor is completed via a diode which receives the necessary forward bias to complete the ground return path when the associated drive transistor is conducting. Consider, for example, the control exercised by transistor Q108. This controls the ground returns for resistor R114 and capacitor C105. When Q108 is cut off, FET switch Q105 is also cut off as a result of the negative bias voltage received through resistor R164. At the same time, diodes CR108 and CR109 are reverse biased by the negative voltage received through resistors R164 and R163. Under this condition, resistor R114 and capacitor C105 are effectively disconnected from the attenuator network since the ground returns for both of these elements are interrupted.

4.208 The fixed bias input to emitter follower Q111 provides a positive voltage at the Q111 emitter when any of the drive transistors is conducting. When Q108 conducts, this positive voltage is applied to its collector circuit as required to provide forward bias for FET switch Q105 and for diodes CR108 and CR109. With Q105 conducting, the ground return of resistor R114 is completed. With CR107 and CR109 receiving forward bias, the ground return of capacitor C105 is completed. Positive excursions of signals coupled through C105 are now shunted to ground through the low forward impedance of diode CR109 while negative excursion are shunted to ground through the low forward impedance of CR108 and capacitor C106.

4.209 In a similar manner, drive transistor Q109 controls the ground return for resistor R115 (by controlling the bias of FET switch Q106) and the ground return for capacitor C108 (by controlling the bias of diodes CR109 and CR110). Likewise, Q110 controls the ground return for resistor R117 (by controlling the bias of FET switch Q107) and the ground return for capacitor C111 (by controlling the bias of diodes CR111 and CR112).

4.210 When the unit is in the local control mode, drive transistors Q108 through Q110 are controlled via steering diodes which supply the low RMT level connected through

the RANGE switch to one or more of the base circuits of the drive transistors. When the RANGE switch is in the PRESET or the 1 position, transistor Q108 receives forward bias through diode CR117 and resistor R157. When the switch is in the .1 position, all three of the drive transistors are off. When the switch is in the 10 position, transistor Q108 receives forward bias via diode CR116 and transistor Q109 receives forward bias via diode CR121. When the switch is in the 100 position, transistor Q108 receives forward bias via diode CR119, transistor Q109 receives forward bias via diode CR122, and transistor Q110 receives forward bias via diode CR123.

4.211 When the unit is in the remote control mode, the RMI input to deck A of the RANGE switch is at the high level and is thus ineffective in supplying forward bias to the base circuits of the drive transistors. Under this condition, this function is assumed by three NAND gates which control the transistor base circuits through another set of steering diodes. These NAND gates are controlled by the true RMI level and by the remote X and Y selection inputs. The resultant selections are summarized below:

X	Y	Q108	Q109	Q110	RANGE Selection
0	0	Off	Off	Off	.1
0	1	On	Off	Off	1
1	0	On	On	Off	10
1	1	On	On	On	100

4.212 When DC input coupling is selected, FET switch Q103 is turned on. This completes a series path from the INPUT A connector, through resistor R104, through FET Q103, and through resistor R119 to the gate element of FET buffer Q112. When AC coupling is selected, FET switch Q104 is turned on and the series path is completed through resistor R105, capacitor C103, FET Q104, and resistor R119. The two FET switches are controlled by drive transistors Q102 and Q101 which have a master/slave relationship. When Q102 conducts, Q101 is held cut off. Under this condition FET Q104 conducts completing the AC input path and FET Q103 is held cut off by the negative bias received through resistor R113. When Q102 is cut off, Q101 conducts. Under this condition, FET Q103 conducts completing the DC input path and FET Q104 is held cut off by the negative bias received through resistor R112. (It is this same negative bias which enables Q101 to conduct.)

4.213 Q102 is controlled via a steering diode from either one of two NAND gates. When the local control mode is selected, the true $\overline{\text{RMT}}$ level selects a NAND gate which receives an input from the local DC-AC switch. When this switch is in the AC position, the signal supplied to the gate is true and Q102 is turned on as required to select the AC input path. When the switch is in the DC position, the gate input is held at a negative level. Thus, in this case, Q102 is cut off and the DC input path is selected. When the remote control mode is selected, RMI is true and the selection control is transferred to the other gate, which receives the remote AC/DC signal. A true level on this line selects the AC input path while a false level selects the DC input path.

4.214 The output signal phase selection which determines whether the counter triggers on the positive or negative slope of the input signal is implemented by selecting either the differential trigger amplifier output which is in phase with the input signal (from the emitter of Q119) or the differential trigger amplifier output which is out of phase with the input signal (from the emitter of Q114) for application to the TRIGGER A line. In either case, the selected signal passes through two NOR gates so that it appears on the TRIGGER A line in phase with the differential trigger amplifier output from which it is obtained. The selection is determined by the status of the signal at the output of NAND gate M105-3. If this signal is high, NOR gate M103-6 is inhibited. At the same time, transistor Q124 conducts and enables NOR gate M103-3. Under this condition, the signal from the emitter of Q119 passes through NOR gate M103-3 and NOR gate M103-8 to the TRIGGER A line. On the other hand, if the signal at the output of NAND gate M105-3 is low, NOR gate M103-6 is enabled. Transistor Q123 is cut off so that NOR gate M103-3 is inhibited. Under this condition, the signal from the emitter of Q114 passes through NOR gate M103-3 and NOR gate M103-8 to the TRIGGER A line.

4.215 When the unit is in the local control mode, NAND gate M105-3 is controlled by the output of NAND gate M105-6 which receives the $\overline{\text{RMT}}$ signal. The second input to this NAND gate is placed at the true level if the Slope switch is in the + position or if the RANGE switch is in the PRESET position.

4.216 When the unit is in the remote control mode, NAND gate M105-3 is controlled by the output of NAND gate M105-8 which receives the RMT signal. The second input to this gate is the remote +/– SLOPE signal.

4.217 When the unit is in the local control mode, the reference input to the base of transistor Q118 of the differential trigger amplifier is determined by the setting of LEVEL potentiometer R144 unless the RANGE switch is in the PRESET position. In this latter case, forward bias for transistor Q120 is supplied through deck B of the switch and through resistor R143. This causes transistor Q120 to conduct and short circuit the input signal from the LEVEL potentiometer to ground so that the differential trigger amplifier receives a 0-volt reference level input.

4.218 When the unit is in the remote control mode, transistor Q120 receives forward bias from the RMT line via resistor R176 and zener diode CR131. Thus, Q120 conducts and inhibits the output of the LEVEL control from reaching the reference input of the differential trigger amplifier. At the same time, the false $\overline{\text{RMT}}$ level removes the forward bias for transistors Q121 and Q122. This bias is supplied through resistor R175 and zener diode CR130 and causes these two transistors to conduct when the unit is in the local control mode. With the unit in the remote control mode so that Q121 and Q122 are cut off, reference voltages can be applied to the differential trigger amplifier from either of two sources. One of these is the analog trigger level control input signal which is applied to terminal E1 and thus reaches the base of Q118 via resistor R179 and resistor R137 when Q121 is cut off.

4.219 The second source of the trigger level control voltage is the output of a 4-bit digital-to-analog converter employing M104 connected as a summing amplifier which sums the signals provided from switch transistors Q124 through Q127. The status of the switch transistors is controlled by the P, N, M, and L digital inputs as required to implement the digital to analog conversion. In addition to the contributions controlled by the switch transistors, which are positive, the summing amplifier receives a negative input through fixed resistor R184 and variable resistor R185. The resistance of R185 is adjusted so as to obtain a zero reference level output from the summing amplifier in response to a digital input of 0111.

4.220 A binary 1 (positive) input to a switch transistor turns on that transistor and shorts out the associated analog input to the summing amplifier. Thus, the maximum positive input is obtained in response to the 0000 digital input. Since the summing amplifier provides an inversion of the input voltages, it follows that 0000 provides the maximum negative triggering level. At the other end of the scale, 1111 provides the maximum positive triggering level. The scaling resistances in the various input branches controlled by the switching transistors are selected to obtain a 1-2-4-8 weighting of the digital inputs with the L input having the weight of 8 and the P input having the weight of 1.

4.221 Dual Program Signal Conditioner.

4.222 This circuit board provides two 50 MHz preamplifier channels and the circuits required to implement either local or remote programming control over the range, triggering level, and coupling parameters of these channels. The circuit board also provides logic which implements either local or remote programming control of the mode, measurement time, and function selections.

4.223 The local and remote control of the preamplifier signal conditioning parameters is identical to that described for the single program signal conditioner in paragraph 4.198 except that two sets of switch inputs and two sets of remote program inputs are involved as required to set separate sets of conditions for the two channels.

4.224 Measurement time and mode control is identical to that provided by the single program signal conditioner. Function control is extended to provide local or remote control of the time interval (T.I.) function. Local and remote control of the separate/common selection is provided. Logic which generates a composite marker signal is provided.

4.225 The function selection is extended to include the T.I. selection by NAND gates M2-11 and M2-3 (sheet 1). Gate M2-11 controls the T.I. selection output line. When local control is selected, gate M2-3 receives the true $\overline{\text{RMT}}$ level. Under this condition, the T.I. output is controlled in accordance with the status of the local T.I. input from the high speed switching logic. When remote control is selected, the status of the T.I. output line is controlled by the decode of the J and K inputs. Specifically, if J is true and K is false, the T.I. output line is placed at the true level.

4.226 The separate/common function is controlled by relay K1. With this relay de-energized, the input to the channel B attenuator is obtained from the INPUT B connector. Since the input to the channel A attenuator is always obtained from the INPUT A connector, it follows that the two channels receive separate inputs. With relay K1 energized, the input to the channel B attenuator is disconnected from the INPUT B connector and is connected to the INPUT A connector. Thus, under this condition, both channels receive the common input that is applied to the INPUT A connector.

4.227 When the local control mode is selected, the true $\overline{\text{RMT}}$ signal enables a gate which receives the signal from the SEP switch. When this switch is in the SEP position, the control input to this gate is true. Under this condition, the emitter of transistor Q3 is held at the positive level so that Q3 is held cut off and K1 remains de-energized. When the SEP switch is placed in the common (COM) position, the emitter of Q3 is grounded. Q3 conducts and K1 is energized.

4.228 When the remote control mode is selected, a gate receiving the remote SEP/COM signal is enabled by the true RMT level. Under this condition, K1 is energized when the SEP/COM signal is false and is de-energized when the SEP/COM signal is true.

4.229 The MARKER OUTPUT signal is controlled by flip-flop M18. This high-speed flip-flop is clocked set by the

true-going transition of the TRIGGER A (MARKER A) signal from channel A and is clocked reset by the inverted false-going transition of the TRIGGER B (MARKER B) signal from channel B. In terms of the input signals to channels A and B, assuming Plus (+) Slope is selected, then the flip-flop is clocked set by positive slope of the input signal to channel A and is clocked reset by the positive slope of the input signal to channel B. The flip-flop output is inverted and amplified by transistor amplifier Q2 to provide a signal which goes negative during the interval when the flip-flop is set.

4.230 Electrical Output Logic.

4.231 This logic provides BCD data outputs for each digit position provided by the unit display. It provides exponent output data which defines the significance of the digit data. It also provides four status signals.

4.232 All output signals are supplied by SN7400, SN7410, or SN7420 positive-logic NAND gates via 39-ohm series output resistors.

4.233 The digit data is supplied from the display latches on the readout card in complement form. It is inverted by the output gates as required to provide positive-true data on the digit output lines.

4.234 The exponent data is a decode of the status of the units counter on the readout board which converts the units count into the exponent of 10 by which the digit output must be multiplied to obtain a frequency value in Hz assuming the decimal point is to the right of the most significant digit. (In the case of a time interval measurement, the exponent is not used. The decimal point is always assumed to be to the left of the least significant digit and the value is always assumed to be in microseconds.)

4.235 The decode of the units count that is performed by the gates in this logic is summarized below:

				J8 - Pin								J8 - Pin			
UD	UC	UB	UA	B	1	3	C	UD	UC	UB	UA	B	1	3	C
0	0	0	0	1	0	0	0	0	1	0	0	0	1	0	0
0	0	0	1	0	1	1	1	0	1	0	1	0	0	1	1
0	0	1	0	0	1	1	0	0	1	1	0	0	0	1	0
0	0	1	1	0	1	0	1	0	1	1	1	0	0	0	1
								1	0	0	0	0	0	0	0

4.236 The four status outputs from the unit are the positive-true signals REMOTE, AUTO, PRINT, and GATE. The $\overline{\text{REMOTE}}$ signal is received in complement form from the mode selection logic and is inverted by the output gate to provide a positive-true signal. A true REMOTE level indicates that the remote control mode has been selected. The AUTO signal is received from a gate on the readout board and is inverted twice by passage through two gates in this logic. A true AUTO level indicates that the AUTO mode is selected and that a RESET is not in progress.

4.237 The $\overline{\text{PRINT}}$ signal is received in complement form from the readout circuit board and is inverted to provide the positive-true PRINT signal. The PRINT signal is true except during those portions of a measurement routine when the contents of the display latches are being updated.

4.238 The $\overline{\text{GATE}}$ signal is received in complement form from the $\overline{\Delta t_T 2}$ line in the high speed switching logic. It is inverted by the output gate to provide a positive-true signal. GATE is true during the intervals when frequency or time interval counts are being accumulated.

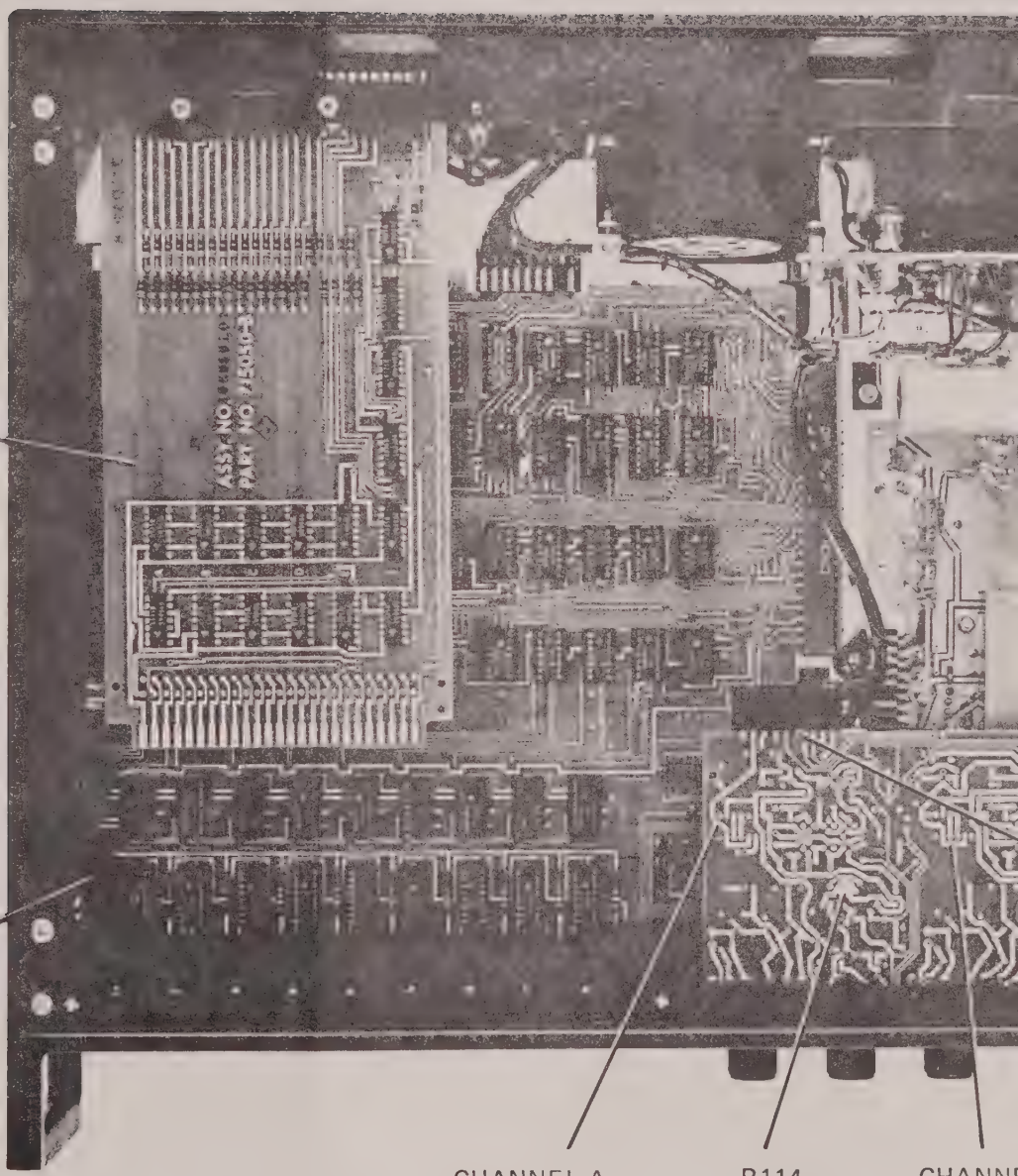


Figure 5-1 Top View

POWER SUPPLY
406043

500 MHz PRESCALER
406048

50 MHz PREAMPLIFIER
DUAL CHANNEL
406044

GROUND
(GROUND
PLANE OF
UNDERSIDE
OF BOARD)

R14
(SEE 6.7)

SECTION 5

SPECIFICATION VALIDATION PROCEDURE

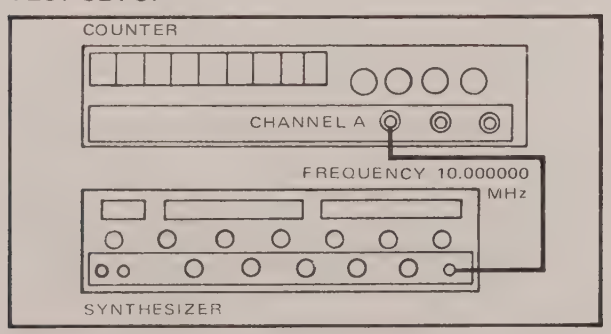
5.1 REQUIRED EQUIPMENT

TYPE	REQUIRED SPECIFICATIONS	SUGGESTED EQUIPMENT
Frequency Synthesizer	Frequency Range - to 10 MHz	Dana 7010
Function Generator	Adjustable Frequency Frequency Range .05 Hz to 10 kHz	Wavetek 110
Signal Generator	Frequency Range 10 MHz 500 MHz Calibrated Attenuator	HP HO 608E
Oscilloscope	Frequency Range 10 MHz	Tek 545/1A2
Time Mark Generator		Tek 184
Frequency Standard	Accuracy 5 x 10^{-10}	HP 106B
Sampling Voltmeter	500 uV sensitivity 10 MHz to 500 MHz	HP 3406

5.2 READOUT

5.2.1 READOUT TUBE CHECK

TEST SETUP



COUNTER CONTROLS

Mode	-	Auto
Measurement Time	-	1
Function	-	Freq. A
Channel A Range	-	Preset

PROCEDURE

Check the display and resolution of least significant digit on the counter by switching through successive digits on the least significant decade of the Frequency Synthesizer. Repeat procedure using more significant decades on the synthesizer.

5.2.2 AUTOMATIC BLANKING

TEST SETUP

Same as 5.2.1.1 with 1 kHz output from synthesizer.

PROCEDURE

Select the various measurement times. The number of digits displayed should be related to the measurement time as follows:

Measurement Time (Seconds)	Number of Digits Displayed
10	8 (9 digits with option 004)
1	8
.1	7
.01	6
.001	5

5.2.3 INACCURATE READING INDICATION

TEST SETUP

Same as 5.2.1.1 except measurement time is .001.

PROCEDURE

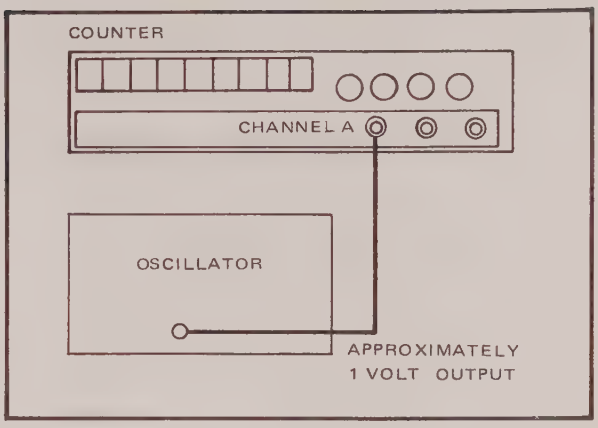
Decrease the frequency output from the synthesizer. When the frequency goes below 250 Hz, display should show all zero's

5.3 FREQUENCY MEASUREMENTS UP TO 50 MHz

5.3.1 FREQUENCY RANGE

5.3.1.1 MINIMUM FREQUENCY RESPONSE

TEST SETUP



PROCEDURE FOR MINIMUM FREQUENCY RESPONSE - DC Coupled

COUNTER CONTROLS

Mode	-	Auto
Measurement Time	-	10
Function	-	Freq. A
Channel A Range	-	1
Channel A Coupling	-	DC
Channel A Level	-	0

Slowly increase oscillator frequency from below .05 Hz until GATE light appears. Wait 20 seconds for a reading. Maximum reading within specifications is 0.05000000 Hz.

PROCEDURE FOR MINIMUM FREQUENCY RESPONSE - AC Coupled

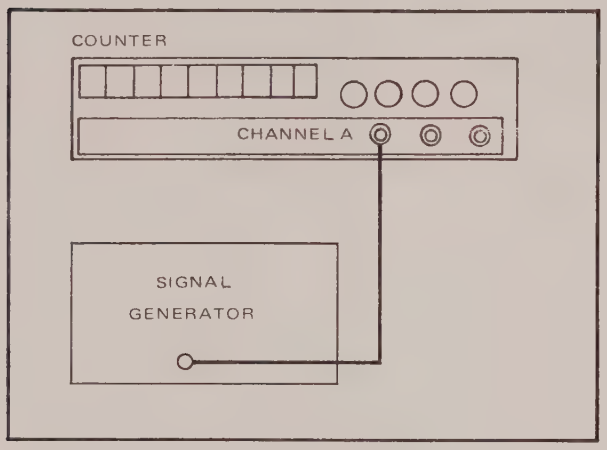
COUNTER CONTROLS

Change measure time to 1 and Channel A Coupling to AC.

Repeat procedure in 5.3.1.1 (b). Maximum reading within specification is 5.000000 Hz.

5.3.1.2 MAXIMUM FREQUENCY RESPONSE

TEST SETUP



COUNTER CONTROLS

Mode	-	Auto
Measurement Time	-	.01
Function	-	Freq. A
Channel Range	-	Preset

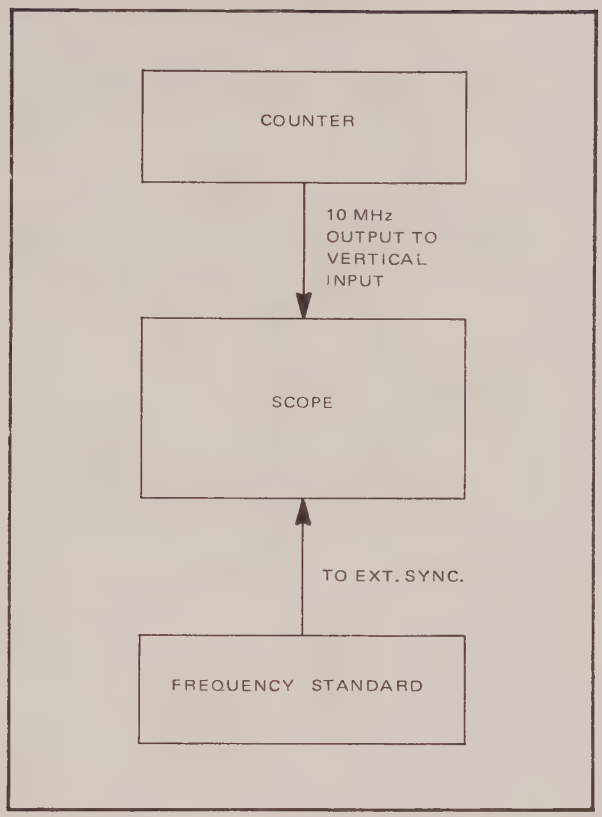
PROCEDURE

Starting at 40 MHz as indicated on the counter display, increase the frequency output from the signal generator until the counter display begins to decrease as the signal generator frequency is increasing or the counter does not make new readings. The minimum frequency at which this foldover occurs should be 50 MHz for the counter to be operating with specifications. Caution: terminate cables with 50 ohms to prevent standing waves.

5.3.2 ACCURACY

5.3.2.1 REFERENCE OSCILLATOR ACCURACY

The frequency accuracy of the internal reference oscillator may be determined by observing the rate of drift of an oscilloscope pattern. To adjust the reference using this technique, the counter, oscilloscope, and frequency standard should be connected as shown below:



If the pattern moves to the right, the counter oscillator frequency is lower than standard frequency being used to trigger the oscilloscope. If the pattern moves to the left, the counter oscillator frequency is high. The reciprocal of the time in seconds for the oscilloscope pattern to move the width of one cycle equals the frequency difference in parts in 10^7 with a 10 MHz input. For example, if the oscilloscope pattern drifts to the left at a rate of one cycle's width every 10 seconds with a 10 MHz input, the counter oscillator frequency is 1 part in 10^8 high. Movement of the pattern may be accurately checked using an oscilloscope with calibrated sweeps by timing the movement of the point at which the oscilloscope trace crosses the base line when horizontal sweep is expanded and vertical gain increased.

TEST SETUP

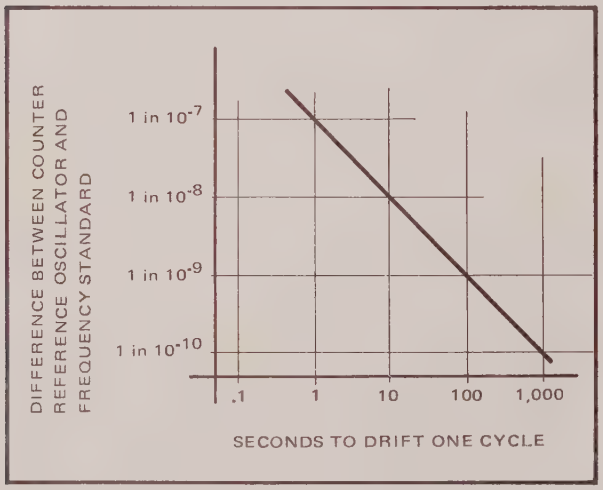
(a) Connect oscilloscope to 10 MHz reference output on counter rear panel.

(b) Trigger oscilloscope externally with a 1 or 5 MHz signal from frequency standard.

(c) Set oscilloscope sweep rate to .02 us per cm. Adjust controls to obtain a presentation of a 5V peak-to-peak non-sinusoidal waveform.

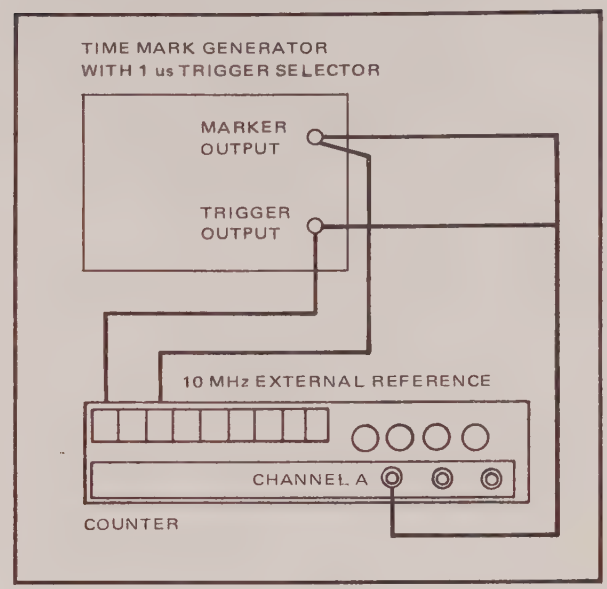
PROCEDURE

Measure the time it takes the oscilloscope pattern to drift the width of one cycle. The difference between the counter reference oscillator and the frequency standard is shown on the graph below:



5.3.2.2 COMPUTING CIRCUITRY

TEST SETUP - Frequency up to 50 MHz



COUNTER CONTROLS

Mode	-	Auto
Function	-	Freq. A
Channel A Range	-	Preset

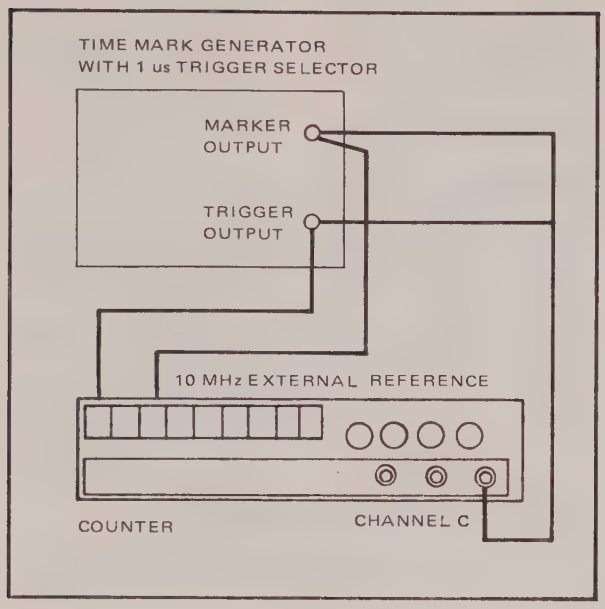
PROCEDURE - Frequency up to 50 MHz

With the following marker selectors, the indication on the counter should be as following for the counter to be within specifications:

COUNTER READING

Marker Selector	One Sec Measurement Time	10 ms Measurement Time	Tolerance (in digits)
1 s	1.0000000 Hz	no reading	
50 ms	20.000000 Hz	no reading	± 2
1 ms	1.0000000 kHz	1.00000 kHz	± 1
50 us	20.000000 kHz	20.0000 kHz	± 2
1 us	1.0000000 MHz	1.00000 MHz	± 1
20 ns	50.000000 MHz	50.0000 MHz	± 5

TEST SETUP - Frequency up to 500 MHz**



COUNTER CONTROLS

Mode	-	Auto
Measurement Time	-	1
Frequency	-	Freq. C

PROCEDURE - Frequency up to 500 MHz**

With the following marker selectors, the indication on the counter should be as follows for the counter to be within specifications:

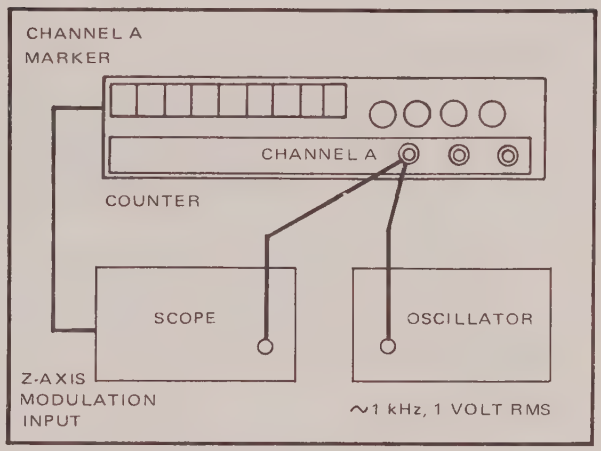
COUNTER READING

Marker Selector	One Sec Measurement Time	10 ms Measurement Time	Tolerance (in digits)
5.0 ns	20.000000 MHz	200.000 MHz	± 2
2.5 ns	400.00000 MHz	400.000 MHz	± 5

5.3.3 TRIGGER ADJUSTMENTS

5.3.3.1 MARKER - Channel A

TEST SETUP



COUNTER CONTROLS

Mode	-	Auto
Measurement Time	-	1
Function	-	Freq. A
Channel A Range	-	1
Channel A Trigger Slope	-	"+"

PROCEDURE

Check to see that trigger marker appears as bright spot on the oscilloscope display of the input waveform. The marker should move in a positive direction on the waveform as the Channel A level control is turned clockwise and in a negative direction as the Channel A level control is turned counter clockwise.

**8120 and 8130 only

5.3.3.2 TRIGGER SLOPE SELECTION - Channel A

TEST SETUP

Same as 5.3.3.1

PROCEDURE

Switch the Channel A trigger slope from "+" to "–". The marker should move from a position on the positive slope of the input waveform to a position on the negative slope of the input waveform.

5.3.3.3 PRESET CONTROL CALIBRATION - Channel A

TEST SETUP - Same as 5.3.3.1

PROCEDURE

Switch the Channel A range control from 1 to Preset. The marker should be on the zero crossing of the input waveform.

5.3.3.4 LEVEL CONTROL CALIBRATION - Channel A

TEST SETUP - Same as 5.3.3.1

PROCEDURE

With the Channel A range switch in 1 and the level control on 0, the marker should be on the zero crossing of the input waveform.

5.3.4 SENSITIVITY

TEST SETUP

COUNTER CONTROLS

Mode	-	Auto
Measurement Time	-	1
Function	-	Freq. A
Channel A Range	-	.1
Channel A Level	-	0

PROCEDURE

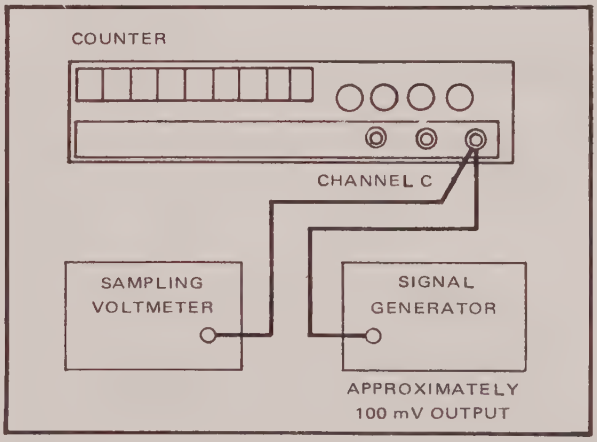
Decrease the output level of the signal generator until the pulse train no longer appears on the oscilloscope. The maximum level at which the pulse disappears should be 10 mV rms for the counter to be operating within specifications.

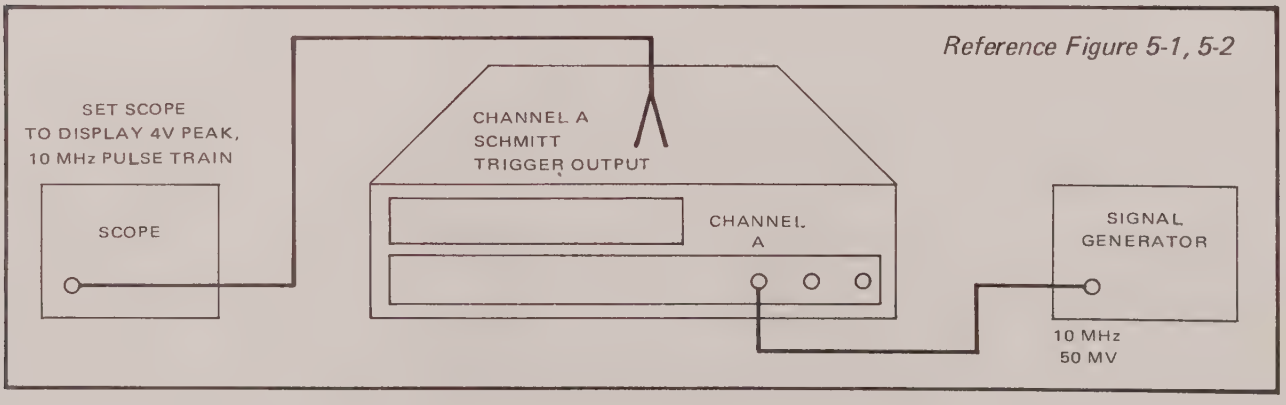
5.4 FREQUENCY MEASUREMENTS TO 500 MHz**

5.4.1 FREQUENCY RANGE

5.4.1.1 MINIMUM FREQUENCY RESPONSE

TEST SETUP




Reference Figure 5-1, 5-2
SET SCOPE TO DISPLAY 4V PEAK, 10 MHz PULSE TRAIN
SCOPE
CHANNEL A SCHMITT TRIGGER OUTPUT
CHANNEL A
SIGNAL GENERATOR
10 MHz 50 MV

**8120 and 8130 only

COUNTER CONTROLS

Mode	-	Auto
Measurement Time	-	.1
Function	-	Freq. C

PROCEDURE

Increase signal generator frequency from below 10 MHz until the red light appears. To be within specification, counter should start reading below 10.000000 MHz.

5.4.1.2 MAXIMUM FREQUENCY RESPONSE

TEST SETUP - Same as 5.4.1.1.

PROCEDURE

Increase signal generator frequency from below 10 MHz until the red light turns off. Minimum reading within specification is 500 MHz.

5.4.2 SENSITIVITY

TEST SETUP - Same as 5.4.1.1.

Signal Generator output frequency - approximately 250 MHz.

PROCEDURE

Decrease the output level of the signal generator until the red light turns off. The minimum level at which the light remains on should be 1 mV rms for the counter to be within specification. Repeat this check with the signal generator output frequency at 10 MHz and 500 MHz.

5.4.3 DYNAMIC RANGE OF AGC

TEST SETUP - Same as 5.4.1.1

PROCEDURE

Decrease the output level of the signal generator until the red light just turns off. Record the level in dBm at which this occurs. Increase the level until the light just turns off. Record this level in dBm. The difference between the two readings should be greater than 60 dB for the counter to be in specification. Repeat this check at 10 MHz and 500 MHz.

5.5 TIME INTERVAL MEASUREMENTS*

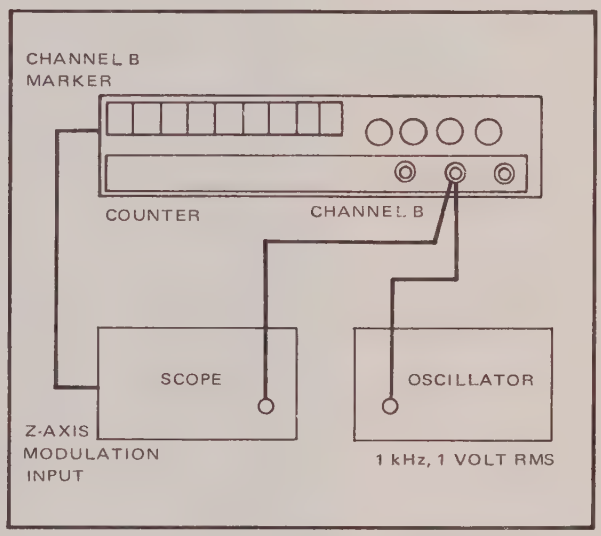
5.5.1 CHANNEL A OPERATION

The checkout procedure for Channel A trigger adjustments and sensitivity is outlined in 5.3.3.

5.5.2 CHANNEL B OPERATION

5.5.2.1 MARKER CHANNEL A

TEST SETUP



COUNTER CONTROLS

Mode	-	Auto
Measurement Time	-	1
Function	-	Time Interval (TI)
Channel B Range	-	1
Channel B Trigger Slope	-	"+"

PROCEDURE

Check to see that trigger marker appears as bright spot on the oscilloscope display of the input waveform. The market should move in a positive direction on the waveform as the Channel B level control is turned clockwise and in a negative direction as the Channel B level control is turned counter clockwise.

*8110 and 8130 only

5.5.2.2 TRIGGER SLOPE SELECTION - Channel B*

TEST SETUP - Same as 5.5.2.1

PROCEDURE

Switch the Channel B trigger slope from "+" to a "–". The marker should move from a positive on the positive slope of the input waveform to a position on the negative slope of the input waveform.

5.5.2.3 PRESET CONTROL CALIBRATION - Channel B

TEST SETUP - Same as 5.5.2.1

PROCEDURE

Switch the Channel B range control from 1 to Preset. The marker should be on the zero crossing of the input waveform.

5.5.2.4 LEVEL CONTROL CALIBRATION - Channel B

TEST SETUP - Same as 5.5.2.1

PROCEDURE

With the Channel B range switch in 1, and the level control on 0, the marker should be on the zero crossing of the input waveform.

5.5.3 SEP/COM SWITCH OPERATION

TEST SETUP

COUNTER CONTROLS

Mode	-	Auto
Measurement Time	-	1
Function	-	Time Interval (TI)
Channel B Range	-	Preset
SEP/COM Switch	-	COM

PROCEDURE

Switch the SEP/COM from COM to SEP. The pulse train should no longer appear on the oscilloscope. Return the switch COM and the pulse train should reappear.

5.5.4 SENSITIVITY

TEST SETUP - Same as 5.5.3 with SEP/COM in COM position.

PROCEDURE

Decrease the output level of the signal generator until the pulse train no longer appears on the oscilloscope. The maximum level at which the pulse disappears should be 100 mV rms.

*8110 and 8130 only

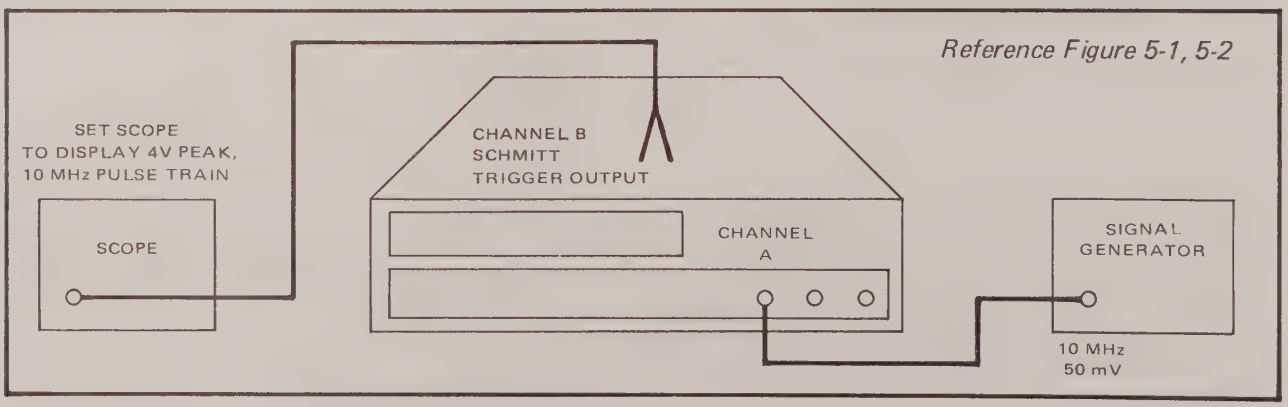


Figure 5-2 Bottom View

SECTION 6

CALIBRATION

6.1 GENERAL

A calibration procedure for all models of the 8100 counter is listed below. Steps pertaining to particular models are so indicated. The adjustments that may be required are:

(a) Power Supply

(b) Reference oscillator

(c) Channel A and B preset trigger levels

(d) Channel A and B trigger level controls

(e) (81X4) Remote programming
Remote Channel A and B trigger level

(f) (8120, 8130) 10 MHz to 500 MHz

1. Frequency response, two adjustments

2. Automatic gain control sensitivity

6.2 EQUIPMENT

TYPE	Required Specifications	Suggested Equipment
Frequency Synthesizer	Frequency Range to 10 MHz	DANA 7010
Oscilloscope	Frequency Range to 10 MHz	TEK 545/1 Hz
Frequency Standard	Accuracy 5×10^{-10}	HP 106B
Voltmeter	DC, Accuracy .1%	DANA 4500
MODELS 8120 and 8130 (Frequency to 500 MHz)		
Signal Generator	10 MHz to 500 MHz Calibrated Attenuator	HP 608E

NOTE: Refer to figures 5.1 and 5.2 for adjustment locations (pages 5-1 and 5-9).

6.3 TOOLS

(a) Insulated blade-type calibration tool

(b) Several interconnecting cables with BNC connectors

(c) 1/16" allen wrench

6.4 PREPARATION

Remove top cover from the counter. Apply power from Variac and allow ten minutes for warm-up. If the counter has options 100, 200, or 300; the following warm-up time is required:

OPTION	WARM-UP TIME
100	24 hours
200	72 hours
300	96 hours

6.5 LINE VOLTAGE REGULATION

6.5.1 Regulation Test and −18 Volt Adjustment

(a) Connect the negative sense of the voltmeter to power supply common (E2). Connect the positive sense to −18 volts, E8 on the power supply board.

(b) Vary the line voltage from 103 volts to 127 volts and observe that the −18 volts changes no more than 80 mvolts. Set Variac for 115 volts.

(c) Adjust R5 on the power supply for −18 volts ± 10 mvolts.

6.6 SIGNAL CONDITIONING – CHANNEL A

6.6.1 Calibration Setup

Connect a 1 KHz signal from the synthesizer to input A of the counter and to the vertical input of the oscilloscope. Connect Channel A marker from the rear panel to the Z-axis input of the oscilloscope. Connect a X10 probe from vertical input B of the oscilloscope to J6 – pin 2 on the preamp connector.

6.6.2 Counter Controls – Channel A

RANGE	PRESET
Trigger Level	0
Slope	+
Coupling	AC

6.6.3 Sensitivity Calibration

(a) Monitor synthesizer output and counter trigger simultaneously on the oscilloscope. Increase synthesizer output from below 100 mvolts until a squarewave trigger is present. Slowly decrease synthesizer output and adjust R14 (R122 on programming models, the pot on the left) to maintain the trigger.

(b) When the input is too low to develop a trigger, increase it slightly and finally adjust R14 (R122 on models with programming). The synthesizer output should be 280 mvolts p-p or less. For 81X4, remote programming, it should be 560 mvolts p-p or less.

6.6.4 Zero Crossover

Set the synthesizer output for 800 mvolts p-p and center the oscilloscope display on the horizontal reference line. Select the 1 range and adjust the trigger level until the marker is on the zero crossover point. Loosen set screws on the knob and rotate it until it indicates zero volts. Tighten set screws.

6.6.5 Remote Programming Zero Crossover (81X4)

Select remote and program for 1 range and zero trigger level. Adjust R185 (the left-rear pot) until the marker is on the zero crossover.

6.7 SIGNAL CONDITIONING – CHANNEL B (8110 and 8130)

6.7.1 Test Setup

(a) Remove connector from Channel A marker and connect to Channel B marker.

(b) Connect vertical input B of the oscilloscope to J6 – pin 4 on the preamp.

6.7.2 Counter Controls – Channel B.

SEP/COM	COMMON
Range	Preset
Trigger Level	0
Slope	+
Coupling	AC

6.7.3 Sensitivity Calibration

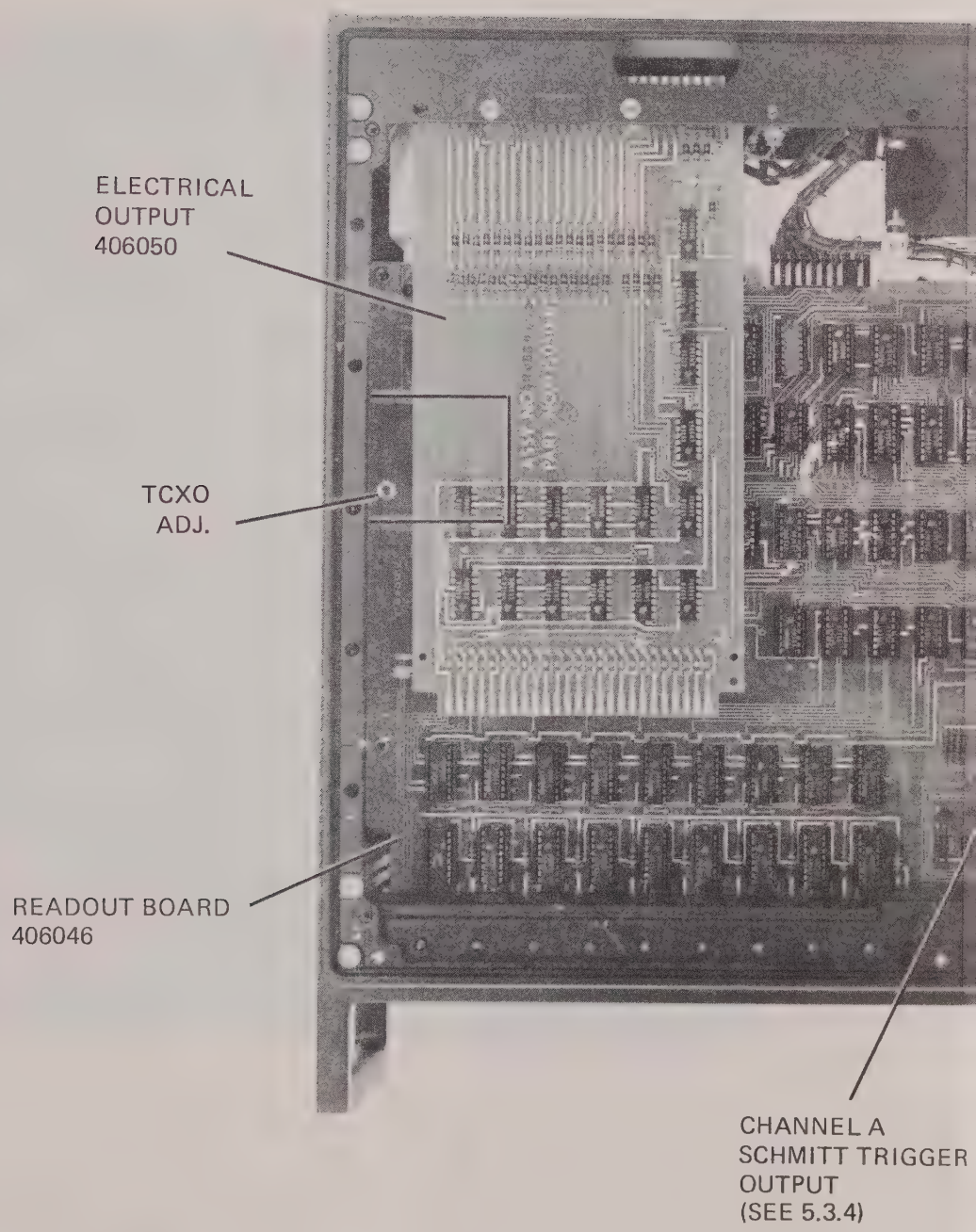
Use same procedure as 6.6.3, but adjust R114 (R322 on programming models, the pot on the right).

6.7.4 Zero Crossover

Use same procedure as 6.6.4.

6.7.5 Remote Programming Zero Crossover (81X4)

Use same procedure as 6.6.5, but adjust R385, the pot at the right-rear of the preamp.


ELECTRICAL
OUTPUT
406050
TCXO
ADJ.
READOUT BOARD
406046
CHANNEL A
SCHMITT TRIGGER
OUTPUT
(SEE 5.3.4)

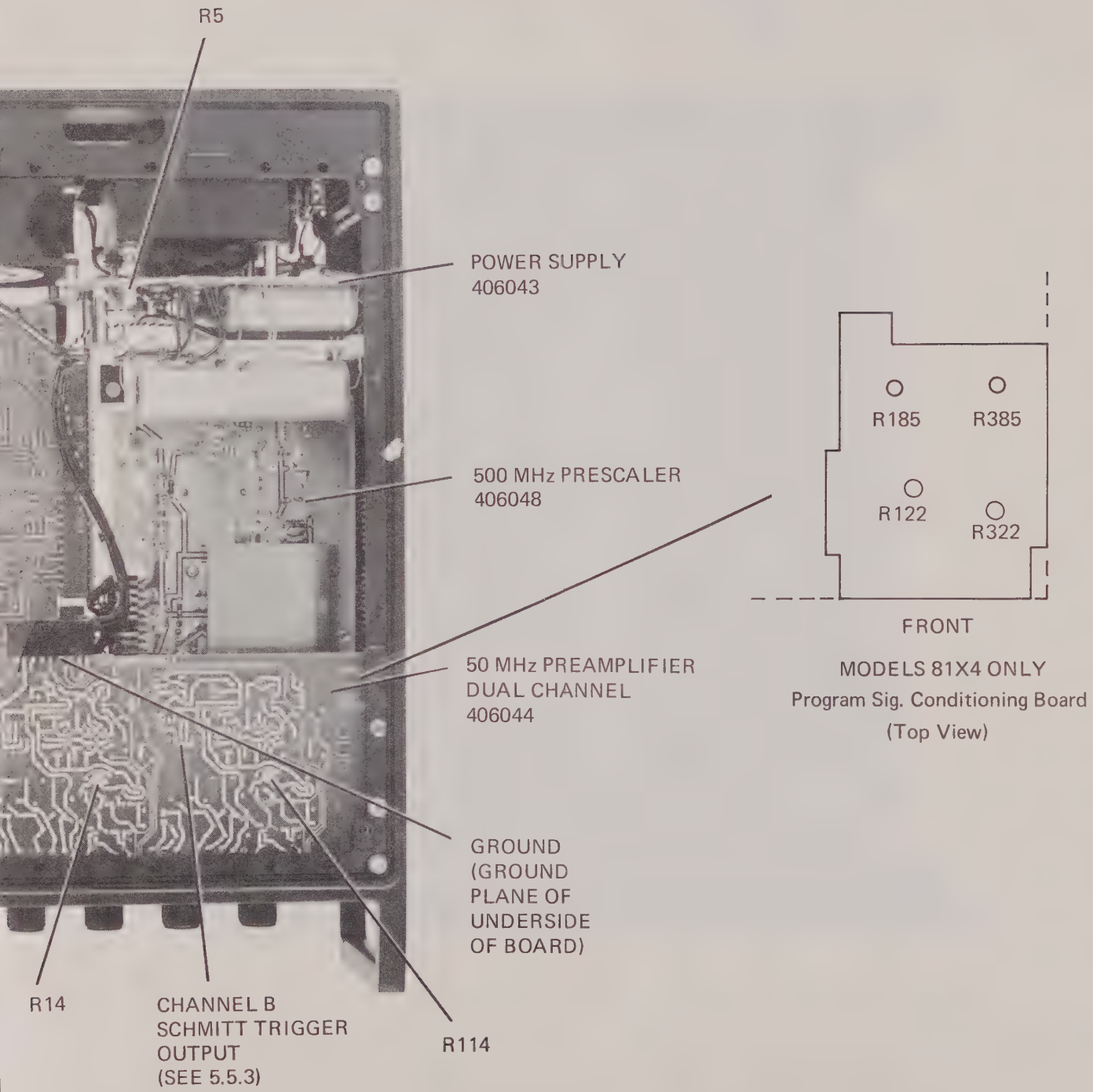


Figure 6.1 - Top View

6.8 REFERENCE OSCILLATOR

6.8.1 Calibration Setup

Connect the 10 MHz reference output from the rear panel of the counter to the vertical input of the oscilloscope. Sync the oscilloscope externally with the frequency standard. Set the scope input attenuator to 1 volt per centimeter and sweep rate to .02 μsec per centimeter.

CAUTION

Use only insulated adjusting tool to calibrate the 100, 200, and 300 option oscillators.

6.8.2 Oscillator Calibration

(a) Adjust the oscillator until the drift rate displayed on the oscilloscope is less than the following:

OPTION	DRIFT RATE
Std	1 cycle width/sec
100	1 cycle width/30 sec
200	1 cycle width/100 sec
300	1 cycle width/200 sec

(b) With standard counter, the top cover must be attached and the oscillator allowed to stabilize after each adjustment to determine the drift rate. With option 100, 200, or 300; the cover screw should be replaced and the oscillator allowed to stabilize before another adjustment is made.

6.9 500 MHz PRESCALER (8120, 8130, 8134).

6.9.1 Calibration Setup

Connect signal generator output to Channel C input of the counter. Remove the bottom cover from the counter.

6.9.2 Counter Controls

Measurement Time	.1 Second
Function	Freq. C

6.9.3 Automatic Gain Control Calibration

Find the sensitivity level with a 10 MHz input by increasing the attenuation from below 500 μvolts to a level where the in-range light just comes on. Note this level and find the sensitivity level at frequencies of every 50 MHz. Note the frequency which takes the greatest input and tune to this frequency. Set the attenuator for 1 mvolt and adjust R64 from fully counterclockwise until the in-range light just comes on.

6.9.4 Frequency Response

(a) Tune the signal generator to 10 MHz with a 1 mvolt output. Adjust R79 fully counterclockwise and then clockwise until the counter reads 10 MHz.

(b) Tune the signal generator to 500 MHz. Adjust R71 for a stable 500 MHz reading. (This adjustment will usually be 3/4 counterclockwise or more.)

(c) Replace the cover and tune the signal generator across all frequencies, observing the counter for the proper readings.

SECTION 7

TROUBLESHOOTING

7.1 INTRODUCTION

This section describes the methods for identifying equipment troubles and determining the specific corrective action that should be taken. Familiarity with the Theory of Operation (Section 4) and with the Use of Operating Controls (Section 3) will make troubleshooting easier.

The goal is to get the unit back on the air as quickly as possible. This requires rapidly defining the trouble in one of four categories:

A. Apparent trouble which is really a faulty control setting or an erratic external signal.

B. Short circuits, or open circuit

C. Analog troubles which require sending Counter to Dana for repair.

D. Digital trouble which can be solved by replacement of plug-in integrated circuits.

Repairs which require replacement of soldered-in components can be accomplished rapidly at the factory. Do not attempt to unsolder components without specific authorization from Dana. Soldering damage is not covered by Dana's warranty.

7.2 APPARENT TROUBLES

8100 Series Counters are complex instruments. It is possible for trouble symptoms to occur that are not equipment malfunctions.

The Counter will not operate if function is incorrectly selected. For instance, if the unknown frequency is connected to Input C and "Freq A" function is selected, there will be no reading. Be sure the "Mode" switch is in "Auto". If "Function" has been changed, press "Reset" to start reading in the new function.

If input voltage range or trigger level are improperly set, Inputs A or B will not operate. Be sure that a measurable signal is present and that controls are set properly for that signal.

When Input C is used, the automatic gain control will inhibit readings of signals which are less than 1 mV, more than 1V, or out of band (below 10 MHz or above 500 MHz). The extreme sensitivity of Input C sometimes requires that unusual precautions be taken. Open leads which might act like an antenna should be avoided. If open leads or probes must be used, it may be necessary to insert a low pass filter at the Counter input to discriminate against unwanted signals received through radiation. Unwanted radiated signals can override the desired signal. The proper operation of Input C can best be verified by connecting a signal generator directly to the Counter through a shielded 50 Ohm cable. Once proper Counter operation has been verified, unwanted external signals can be attenuated with a low pass filter.

The constant percentage of reading error (always 1×10^{-7} of reading for a one second measurement time) of an automatic counter may be confusing. Regardless of measurement time or unknown frequency, this error will be indicated as a flicker of between 1 and 9 digits in the extreme right hand window. For instance, at a reading of 500 kHz, 5 MHz, or 50 MHz, the right hand digit will be flickering by five counts (from 0 to 5; from 1 to 6, etc.) If the reading were 4 MHz, the flicker would be four digits, etc. This multi-digit flicker in the least significant place is normal, as long as the amount of flicker is equal to the reading of the most significant digit.

7.3 VISUAL CHECK FOR SHORTS AND OPENS

A possible source of trouble will be short-circuits which disable portions of the instrument or load down the power supply, or both. Often these short-circuits can be located by visual inspection. A quick visual check of the instrument with the covers removed may reveal foreign metal parts, frayed cable braid, etc. which can be easily cured. Visual checks can be more meaningful after trouble has been localized.

Open circuits can also be located visually. Examine connectors and wire harnesses for obvious breakage.

7.4 TROUBLESHOOTING FROM FRONT PANEL SYMPTOMS

Identify the trouble in one of the following categories; then refer to the appropriate paragraph and follow the suggested procedure.

READOUT PROBLEMS	7.5
FREQUENCY A PROBLEMS	7.6
TIME INTERVAL PROBLEMS*	7.7
FREQUENCY C PROBLEMS**	7.8
DIGITAL PROBLEMS	7.9

7.5 READOUT PROBLEMS

7.5.1 If the readout tubes do not light, a gross failure is indicated.

7.5.1.1 Check line fuse. If OK,

7.5.1.2 Measure line voltage. If OK,

7.5.1.3 Check high voltage supply. Remove top cover. Turn off power and disconnect 9 pin connector at rear of readout board (careful—when power is on, 220 Volts are on this connector). Turn power on and measure high voltage supply. It is the single red wire on the power supply card (right rear). This voltage should be greater than +220 Volts with respect to common (plain black wires on power supply card).

If high voltage is not present check harness, then, return Counter to Dana.

If high voltage is present, reconnect readout board and recheck. If it loads down, locate and eliminate short on readout board. If it doesn't load down, locate and eliminate open circuit.

7.5.1.4 If tubes still do not light, return Counter to Dana.

7.5.2 If all readout tubes blur, loading of the +5 Volt supply is indicated.

7.5.2.1 Check the +18, -18, and +5 supplies as labeled on the power supply board. DO NOT ADJUST TRIMPOT. By selectively disconnecting boards from the power supply, locate the module with the short and eliminate it. Note that the +5 supply is derived from the +18, so that loading on +18 supply can affect the +5.

7.5.2.2 If the reason for low voltage can not be determined, or if the power supply is low even when unloaded, return the Counter to Dana.

7.5.3 If trouble appears in only one readout tube, a bad driver or a bad readout tube is indicated.

7.5.3.1 Driver I.C.'s are 7441's in Row F directly behind readout. Swap driver behind bad readout with neighboring driver. If trouble moves with driver, replace it.

7.5.3.2 If trouble stays when driver is moved, replace readout tube.

7.5.3.3 If trouble persists, inspect board near tube for shorts.

7.5.4 Units Readout Bad

7.5.4.1 If "usec" does not read out in T.I. function, return to Dana.

*8110 and 8130 only
**8120 and 8130 only

7.5.4.2 If "MHZ" does not readout properly, replace C3‡.

7.5.4.3 If "KHZ" does not readout properly, replace C3‡.

7.5.4.4 If "HZ" does not readout properly, replace B4‡.

7.5.4.5 If "Gate" does not readout properly, replace B4‡.

7.5.4.6 If any decimal point fails to indicate, replace C2‡ or C3‡.

7.5.4.7 If decimal point and units display fail to indicate replace C2‡, C4‡, C5‡, or C10‡.

7.6 FREQUENCY A PROBLEMS

7.6.1 Be sure input signals and controls are correct.

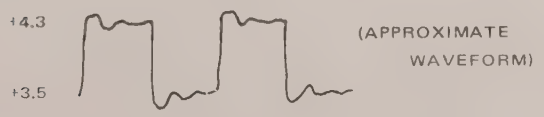
Function	"Freq. A"
Range	"1"
Trigger level	"0"
AC/DC	"AC"
Polarity	"+"

Input signal 200 kHz (approx.) 1 V rms sine wave to Input A.

Try moving level control over range. If trigger level is out of adjustment refer to 6.6.1.

7.6.2 If Freq. A does not function, connect a 10 MHz - 500 MHz, 0.1 Volt RMS signal to Input C.

7.6.3 If Freq. C works, trouble is indicated in A channel. With 200 kHz input to A, remove cover and connect scope to Channel A output (Pin 2 – second from left – of connector at rear of signal conditioning board). This output should be a MECL square wave:



For future reference, place SEP/COM switch in "COM" and check channel B on Pin 4. Set B controls same as "A". (Should also be MECL square wave)

7.6.3.1 If A output is good, proceed to digital problem section, (7.9).

7.6.3.2 If A output is bad:

(a) Replace A output IC (MC 1010—on underside at left) and recheck output.

(b) Check low voltage power supply on connector.

Pin 1	-	Ground
Pin 3	-	+18
Pin 8	-	-18
Pin 9	-	+5

If power supply is bad, follow procedure for 7.5.2.

(c) If none of above results in output coming on, return Counter to Dana.

7.6.4 If frequency C does not work, proceed to Digital Problems, (7.9).

7.7 TIME INTERVAL PROBLEMS

7.7.1 Be sure input signals and controls are correct. Use same set-up as 7.6.1 except:

Function	"T.I."
SEP/COM	"COM"

7.7.2 If T.I. does not function, follow exact procedure of 7.6.3 to check input/output.

7.7.2.1 If A and B outputs are good, proceed to digital troubles.

‡These are IC addresses by row and column on the readout board. Addresses are plated on the board.

7.7.2.2 If either A or B output is bad,

(a) Replace output I.C., on underside of board, and re-check. (notch on I.C. faces rear)

(b) Check low voltage power supply as in 7.6.3.2.

(c) If none of above results in outputs coming on, return Counter to Dana.

7.8 FREQUENCY C PROBLEMS

7.8.1 Connect a signal between 10 and 500 MHz of about 0.1V RMS amplitude to input C with function switch to "Freq. C".

7.8.1.1 If no reading occurs with "in range" light on, proceed to digital problems. (7.9)

7.8.1.2 If no reading occurs and "in range" light is out proceed to 7.8.2.

7.8.2 Connect a signal to Input A (see 7.6.1)

7.8.3 If A works, reconnect input to C, remove top cover, and put scope on output at Pin 1 of output connector of RF board (rear-most pin). This should be a MECL waveform with 60% duty cycle (See 7.6.3).

7.8.3.1 If output is bad, check low voltage power supply (7.5.2)

7.8.3.2 If output cannot be obtained return Counter to Dana.

7.8.4 If A doesn't work either, proceed to digital problems. (7.9)

7.9 DIGITAL PROBLEMS

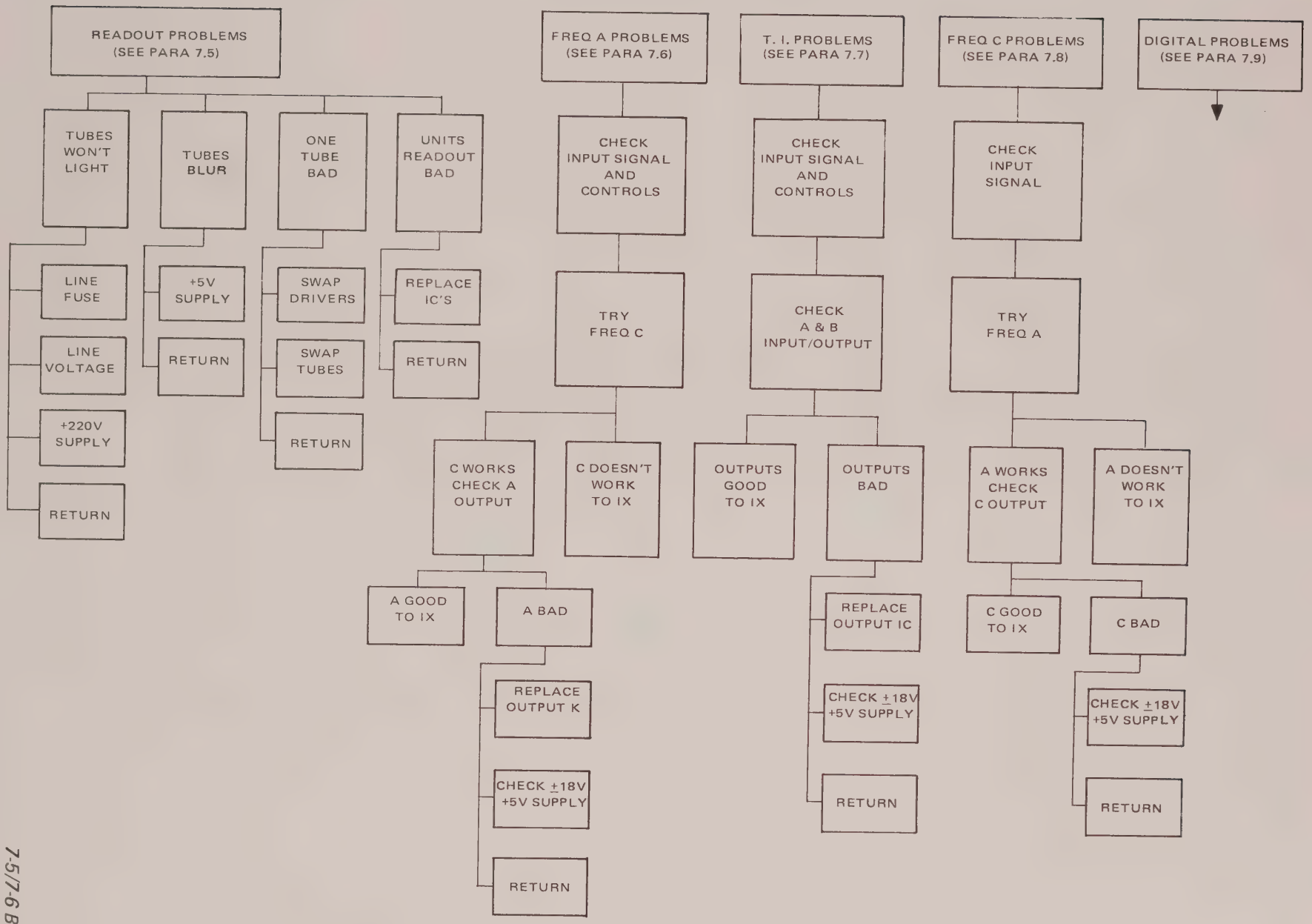
Digital troubles can be solved by combining symptom diagnosis with trial and error IC replacement. An understanding of the block diagram (Theory of Operation Section) combined with Common sense interpretation of trouble symptoms will produce the best results.

The table below isolates troubles to a zone of the Counter. Then selective IC replacement will effect the cure. Failures are more likely in the complex IC's (Adders-7483, Registers-7491, 7496).

IMPORTANT

Integrated circuits can be removed from their sockets and replaced easily and without damage if the correct procedure is used. The use of special tools is not necessary. To remove an IC, place both thumbs on top of IC and both index fingers at the ends of the IC. Gently rock the IC upward in small steps. Do not "pop" it out in one motion. To replace an IC, be sure the notched end points the same direction as the other ICs on the board. Straighten any bent pins. Align the pins on the IC with the holes in the socket and press the IC in firmly using one or two fingers.

TROUBLESHOOTING TREE



TROUBLESHOOTING GUIDE

CONDITIONS		SYMPTOMS	ZONES
Function	Freq A	Gate light fails to come on when "Reset" pushed	1, 4 (Check logic signal at K7, Pin 12
Signal	1 Volt RMS, 1 kHz		
Input	A		
Mode	Hold		
Measurement Time	1		
Range	Preset	Gate light stays on indefinitely, when "Reset" pushed	1, 5
		Gate stays on for 1 second after "Reset" but	
		(a) Readouts all indicate "0"	7, 8, 9
		(b) Leftmost Readout blurs, others "0"	7, 10
		(c) Random numbers	6, 7
		(d) Readouts all indicate same number	7, 8
		(e) Readout indicates less than 200 Hz	2
		(f) Multiple decimal points	6, 7
		(g) Error in units readout	7
		(h) Readout correct, but shifted right	7
		(i) Readout is about 1 Hz high, and changes to about 10 Hz high when measurement time changed to 0.1 second and "reset" pushed	6
		Gate stays on for about 4 seconds after "Reset". Readouts "0"	1, 3
		Gate stays on for more than 10 seconds following "Reset"	3
Function	Freq A		
Signal	10 MHz Ref. Out	After "Reset" gate is on for about 1 second, readout is between 10.000003 MHz and 10.000200 MHz]	2, 5
Input	A		
Mode	Hold		
Measurement Time	1		
Range	Preset		

CONDITIONS		SYMPTOMS	ZONES
Function	Freq A		
Signal	1 Volt RMS, 1 kHz	Gate is on for 1 second, but fails to Restart	11
Input	A	Restart	
Mode	Auto		
Measurement Time	1	Readout appears correct, except for one tube, which	
Range	Preset	(a) is blank	13, 14
		(b) is blurry	12, 14
		(c) shows multiple numbers	12, 13, 14
		(d) will only display one of the following series 1, 3, 5, 7, 9 2, 3, 6, 7 4, 5, 6, 7 8, 9	12, 13
		(e) will not dipslay one of above series	12, 13
Function	Freq A		
Signal	1 Volt RMS, 1 Hz to 10 kHz	As input is varied from 1 Hz up readout may indicate zero below 200 Hz	1
Input	A		
Mode	Auto	Readout is grossly in error up to 5 kHz Accuracy improves above 5 kHz	
Measurement Time	1		
Range	Preset		
Function	TI	Must work in Freq A first. After pushing "Reset"	
Signal	1 Volt RMS, 1 kHz		
Input	A	(a) Readouts all "0"	8, 9
Mode	Hold		
Measurement Time	1	(b) Readouts all same number	8
"A" Range	1		
"A" Level	0	(c) Readouts appear to be continuously counting	8, 9
"A" AC/DC	AC		
"A" +/–	+		
SEP/COM	COM		
"B" Controls except +/– which is "–"	Same as "A"		

CONDITIONS		SYMPTOMS	ZONES
Function	Freq C	Must work in Freq A first	
Signal	0.1 V RMS, any fixed freq. between 10 MHz and 500 MHz	Gate doesn't come on, readouts all "0"	1 - Check signal at K7, Pin 10
		Readout is correct, but decimal point is shifted one place	10
Input	C		
Mode	Auto		
Measurement Time	1		
		Won't lock on external Ref.	4
		Internal Ref. Out Missing	4

DIGITAL ZONES

ZONE 1 - Input Arming

Address*	Type
K6	1010
K7	1007
A2	7420
C3	7474
C2	1022
L6	1022
L5	7402
B3	7402
B4	7400
L7	7402

ZONE 2 - Dump

A4	7474
A7	7474
A10 Readout	7400
E5	7402
L5	7402
E4	7400
J4	7400
F4	7400
K4	7400
B5	7402
B7	7400
D5	7410
D4	7400
C10 Readout	7400
A9 Readout	7402

ZONE 3 - Measurement Time

M6	7430
E6	7400
D3	7400
M7	7400
B4	7400

ZONE 4 - Timing

Address*		Type
B9	Readout	7400
B10	Readout	7496
A6	Readout	7474
A7	Readout	7420
A5	Readout	7400
A9	Readout	7402
A10	Readout	7400
C10	Readout	7400
B5	Readout	7400
B6	Readout	7400
A8	Readout	7402

ZONE 5 - Time Base Register

M2	7491
M3	7491
L3	7491
L2	7491
K1	7483
K5	7490
J5	7490
A7	7474
G5	7474
J1	7474
J2	7474
J3	7474
K2	7474
K3	7474
H5	7402
L1	7400
M1	7400
L4	7400
M5	7400
C5	7402
F5	7402

ZONE 6 - Frequency Register

Address*	Type
H2	7491
H3	7491
G2	7491
G3	7491
F1	7483
H1	7483
H4	7490
F7	1013
G7	1013
H7	1013
J7	1013
C3	7474
C4	7474
J1	7474
E2	7474
E3	7474
F2	7474
F3	7474
D4	7400
D3	7400
G4	7400
E5	7402
E1	7410
G1	7400
F5	7402

ZONE 7 - Arithmetic Unit

B3	Readout	7490
B2		7400
B1		7400
C1		7400
D1		7400
D2		7400
A6		7402
A5		7400
B7		7400

DIGITAL ZONES (Continued)

ZONE 7 - Arithmetic Unit

B5		7402
C5		7402
D6		7400
E7		7400
B5	Readout	7400
E5		7402
E6		7400
A2		7420
B1		7410
E1		7410
C6		7474
D7		7474
C7		7474
D5		7410

ZONE 8 - Logic Switch

B2	Readout	7400
C1	Readout	7400
B1	Readout	7400
B4	Readout	7400
C6	Readout	7402

ZONE 9 - Time Interval

A6		7402
B5		7402
D10	Readout	7400
C10	Readout	7400
C9	Readout	7400
C8	Readout	7400
C7	Readout	7400
C6	Readout	7402
B6		7474
A5		7402

ZONE 10 - Frequency Digit Selector

B7	Readout	7496
B8	Readout	7496
B6	Readout	7400
B5	Readout	7400
D10	Readout	7400
C10	Readout	7400
C9	Readout	7400
C8	Readout	7400
C7	Readout	7400
D6	Readout	7402

ZONE 11 - Automatic Restart

B5		7402
B7		7400
B3		7402
C7		7474
A5		7474

ZONE 12 - Storage

E11	Readout	7475
E12	Readout	7475
E13	Readout	7475
E14	Readout	7475
E15	Readout	7475
E16	Readout	7475
E17	Readout	7475
E18	Readout	7475
E19	Readout	7475
D6		7402
D7	Readout	7410
D8	Readout	7410
D9	Readout	7410

ZONE 13 - Decoder/Drivers

F11	Readout	7441
F12	Readout	7441
F13	Readout	7441
F14	Readout	7441
F15	Readout	7441
F16	Readout	7441
F17	Readout	7441
F18	Readout	7441
F19	Readout	7441

ZONE 14 - Dipslay Tubes

V8	Readout	Tube
V9	Readout	Tube
V3	Readout	Tube
V4	Readout	Tube
V5	Readout	Tube
V6	Readout	Tube
V7	Readout	Tube
V1	Readout	Tube
V2	Readout	Tube

ZONE 15 - Units Display

C5	Readout	7490
C4	Readout	7442
C10	Readout	7400
B4	Readout	7400
C2	Readout	7410
C3	Readout	7410
D7		7474
E7		7400

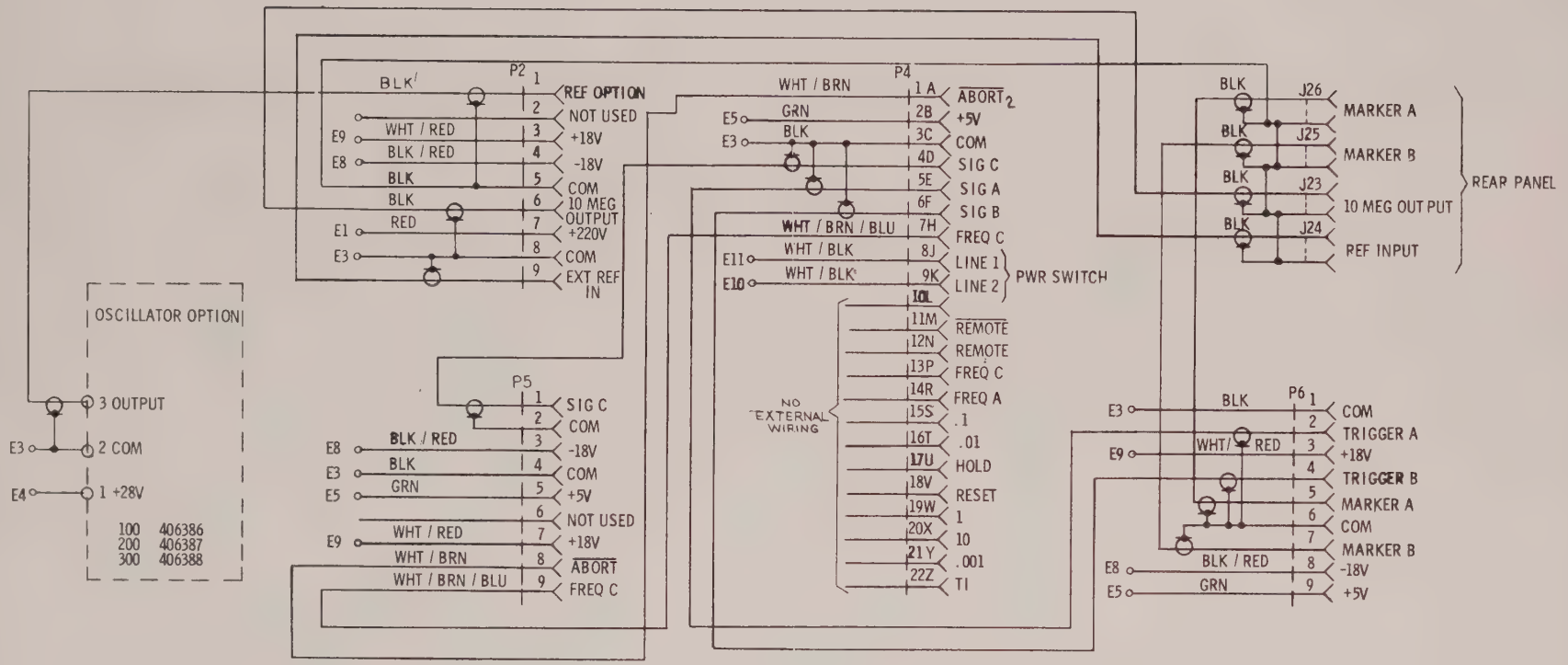
*These are addresses plated on the circuit board by row and column. Unless otherwise noted, they are on the switch board, accessible by removing bottom cover. Where "Readout" is specified address is on readout board, accessible by removing top cover.

SECTION 8

DRAWINGS

8.1 DRAWINGS

Assembly Explosion - 8100		406531
Schematic Interconnection 8130		721474
PCB Assembly Power Supply		406043
Schematic Power Supply		721043
PCB Assembly Units Display		406055
PCB Assembly Readout 8 Digit		406046
PCB Assembly Readout 9 Digit		406378
Schematic Readout		721046
PCB Assembly High Speed Switching		406081
Schematic High Speed Switching		721081
PCB Assembly 50 MHz Preamp Single	Non-programmable Units	406057
Schematic 50 MHz Preamp Single		721057
PCB Assembly 50 MHz Preamp Dual		406044
Schematic 50 MHz Preamp Dual		721044
PCB Assembly 500 MHz Prescaler		406048
Schematic 500 MHz Prescaler		721048
PCB Assembly Program Signal Conditioner - Single	Programmable Units	406047
Schematic Program Signal Conditioner - Single		721047
PCB Assembly Program Signal Conditioner - Dual		406049
Schematic Program Signal Conditioner - Dual		721049
PCB Assembly Electrical Output		406050
Schematic Electrical Output		721050
Dimensional Outline 8100 Series		730350



NOTES: UNLESS OTHERWISE SPECIFIED

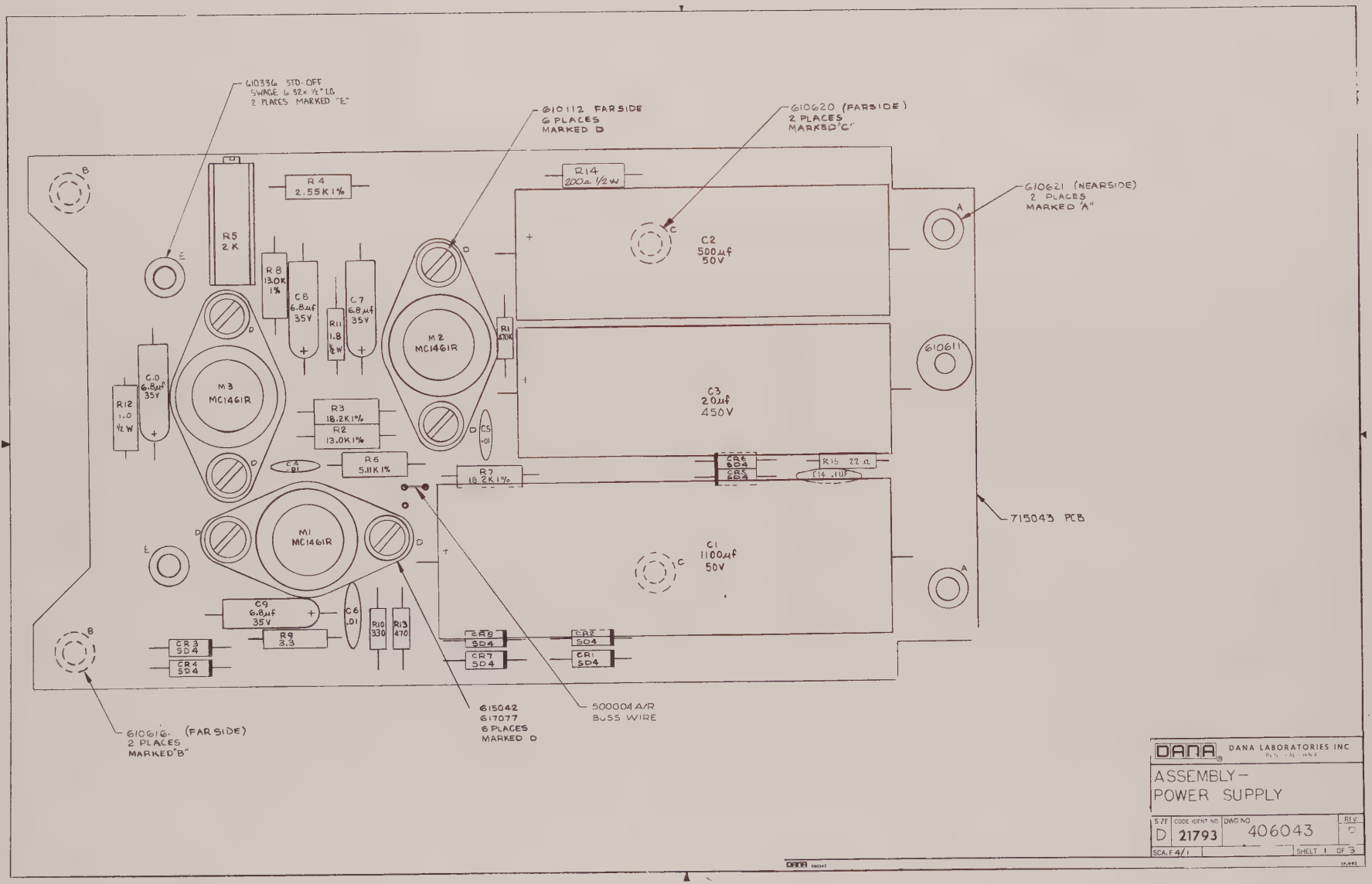
DANA DANA LABORATORIES INC.
IRVINE, CALIFORNIA

SCHEMATIC–
INTERCONNECTION
8130

SIZE	CODE IDENT NO.	DWG NO.	REV
C	21793	721474	B

SCALE —— SHEET | OF |

DIETERICH POST CLEARPRINT 1080

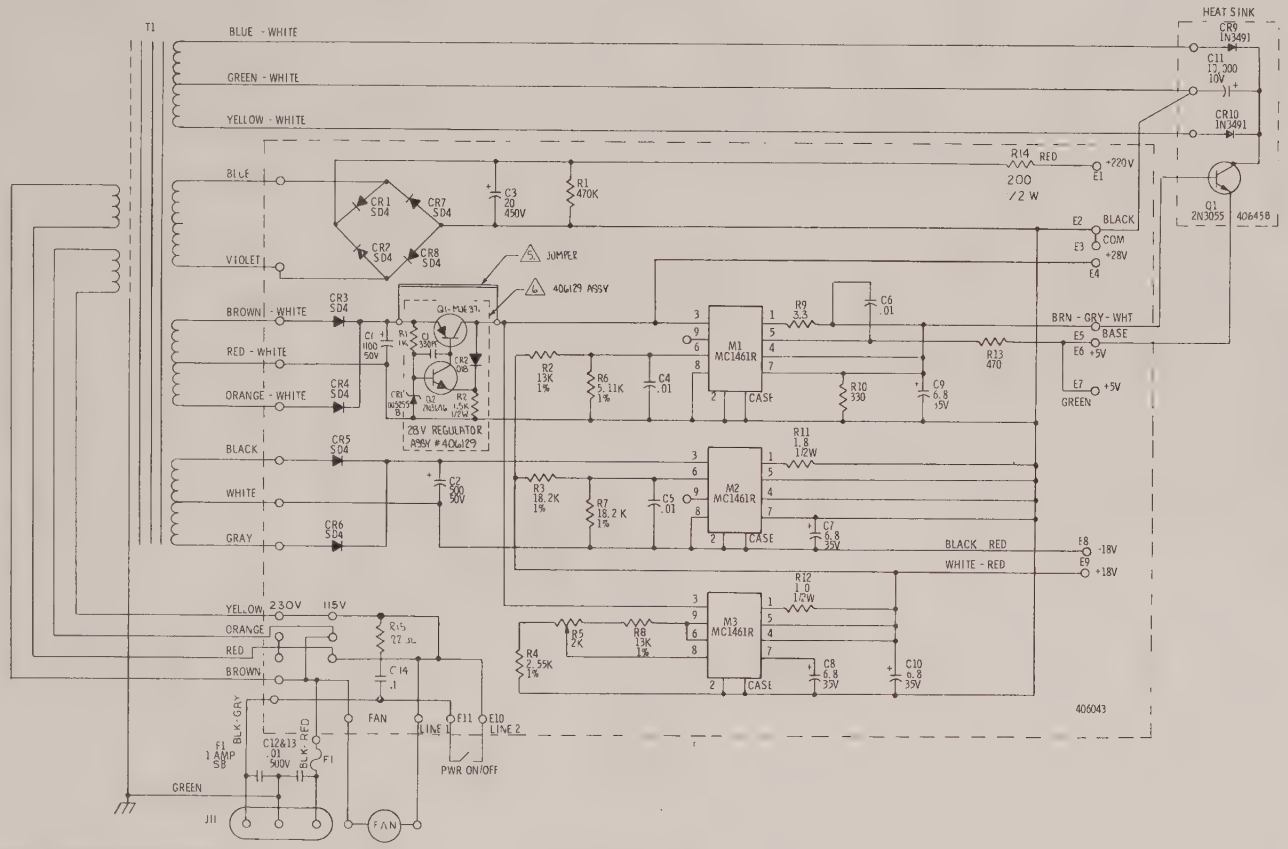


DANA DANA LABORATORIES INC

ASSEMBLY—
POWER SUPPLY

SIZE	CODE IDENT NO	DWG NO	REV
D	21793	406043	D

SCALE 4/1 SHEET 1 OF 3



HIGHEST REFERENCE DESIGNATOR

C	CR	R	F	M	T	Q
14	10	15	1	3	1	1

NOTES UNLESS OTHERWISE SPECIFIED

1. ALL RESISTOR VALUES ARE IN OHMS 5%, 1/4W
2. ALL 1% PRECISION RESISTORS ARE RN60D
3. REFERENCE SCHEMATIC 721474 FOR MODEL 8130
4. ALL CAPACITOR VALUES ARE IN uF

⚠5 JUMPER INSTALLED ON STANDARD USAGE PWR. SUPPLIES.

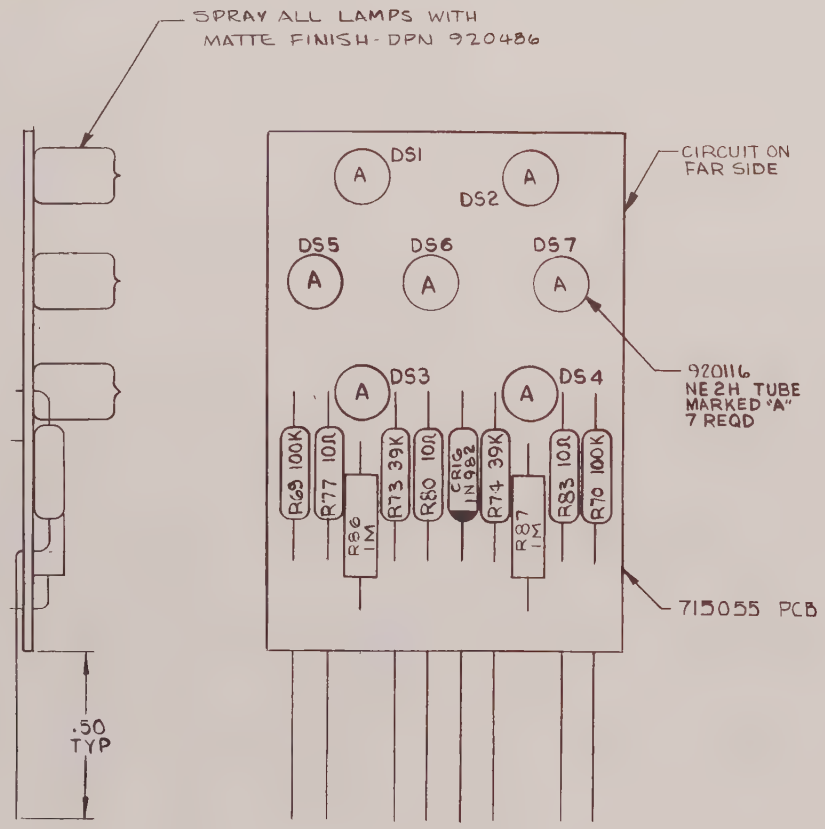
⚠6 406129 PCB ASSY 28V REGULATOR USED WITH OPTIONS 100, 200, 300. JUMPER IS DELETED.

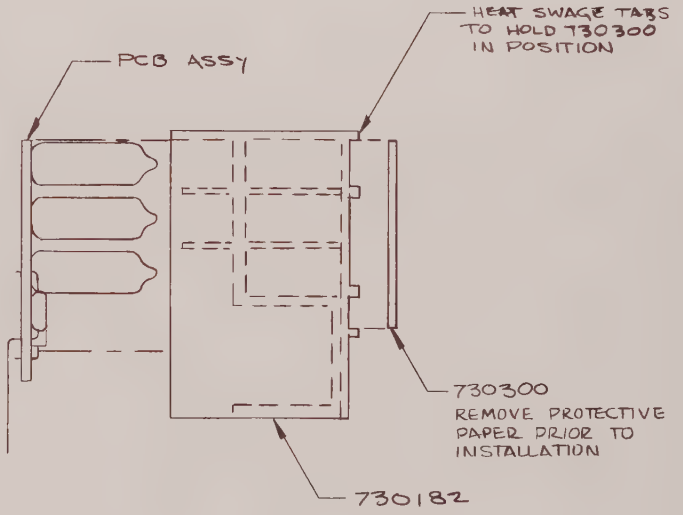
DANA DANA LABORATORIES INC. IRVINE, CALIFORNIA

SCHEMATIC- POWER SUPPLY

SIZE	CODE IDENT NO	DWG NO	REV
D	21793	721043	J

SCALE —— SHEET 1 OF 1





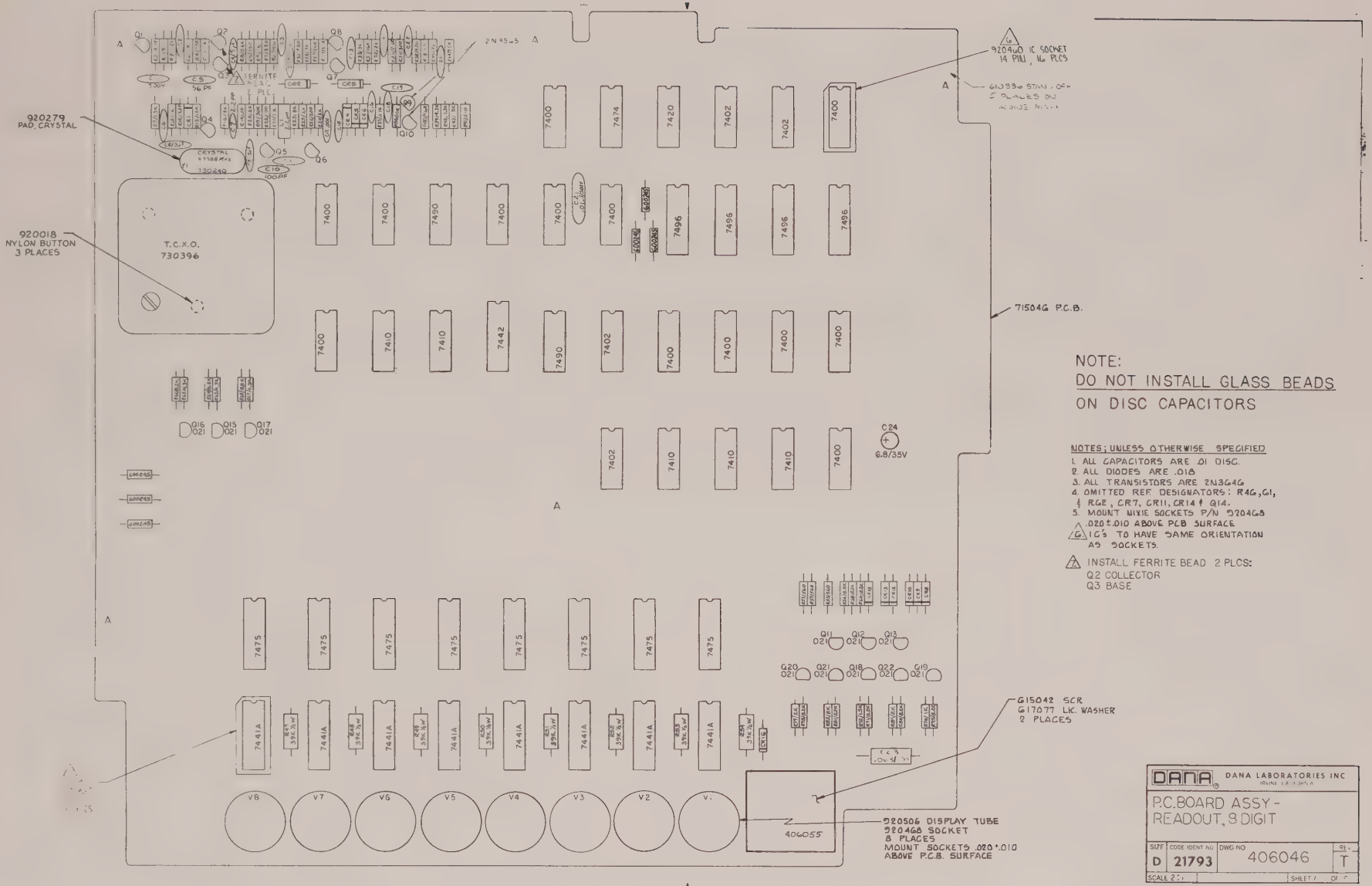
1. REF SCHEMATIC 721046
NOTES: UNLESS OTHERWISE SPECIFIED

DANA LABORATORIES INC.
IRVINE, CALIFORNIA

ASSY-UNITS DISPLAY

SIZE	CODE IDENT NO.	DWG NO.	REV
C	21793	406055	L

SCALE 4/1 SHEET 1 OF 2



NOTE:
DO NOT INSTALL GLASS BEADS
ON DISC CAPACITORS

NOTES; UNLESS OTHERWISE SPECIFIED
1. ALL CAPACITORS ARE .01 DISC.
2. ALL DIODES ARE .018
3. ALL TRANSISTORS ARE 2N3646
4. OMITTED REF. DESIGNATORS: R46, G1, R62, CR7, CR11, CR14 & Q14.
5. MOUNT NIXIE SOCKETS P/N 920468 .020±.010 ABOVE PCB SURFACE
6. ICS TO HAVE SAME ORIENTATION AS SOCKETS.

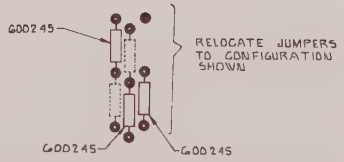
INSTALL FERRITE BEAD 2 PLCS:
Q2 COLLECTOR
Q3 BASE

DANA LABORATORIES INC
IRVINE, CALIFORNIA

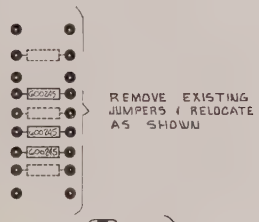
P.C. BOARD ASSY -
READOUT, 8 DIGIT

SIZE	CODE IDENT NO	DWG NO	REV
D	21793	406046	T

SCALE 2:1 SHEET 1 OF -

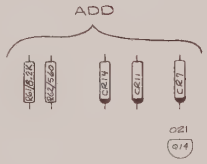


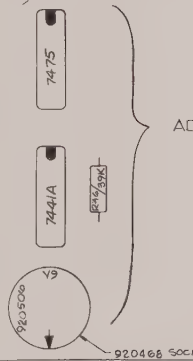
715046 PCB



REMOVE EXISTING JUMPERS & RELOCATE AS SHOWN

ADD





ADD

NOTES:

1. ALL DIODES ARE 018

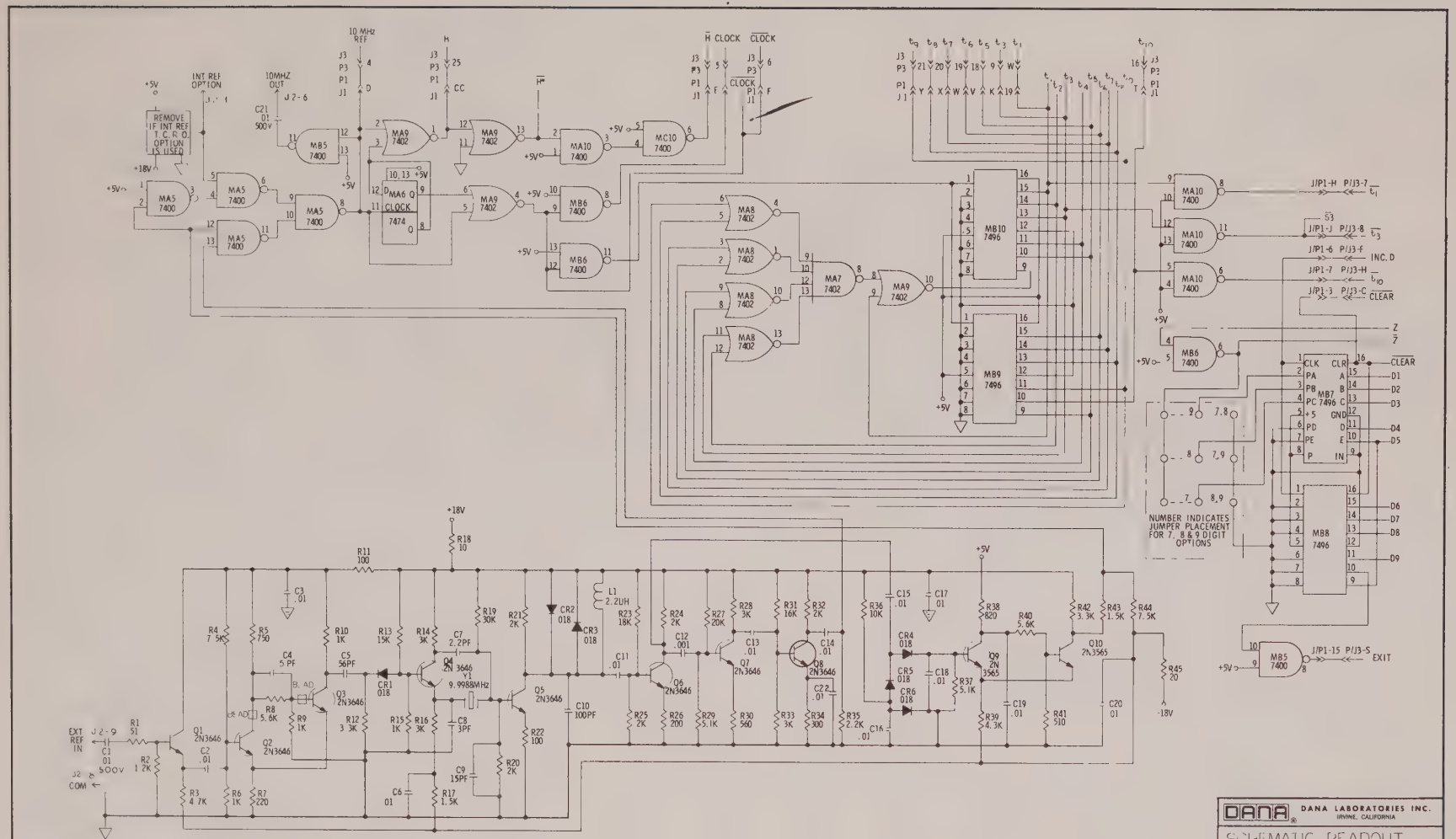
DANA DANA LABORATORIES INC IRVINE CALIFORNIA

ASSEMBLY

READOUT 9-DIGIT

SIZE	CODE IDENT NO	DWG NO	REV
D	21793	406378	L

SCALE 2:1 SHEET 1 OF 2



4. ALL CAPACITOR VALUES ARE IN UF
3. NO BOARD CONNECTION EXISTS BETWEEN ⏚ AND ⏚
2. PIN 7 IS GROUND AND PIN 14 IS +5V FOR 7400, 02, 10, 20, 74 I.C.S
1. ALL RESISTOR VALUES ARE IN OHMS AND ARE 1/4 W. 5%

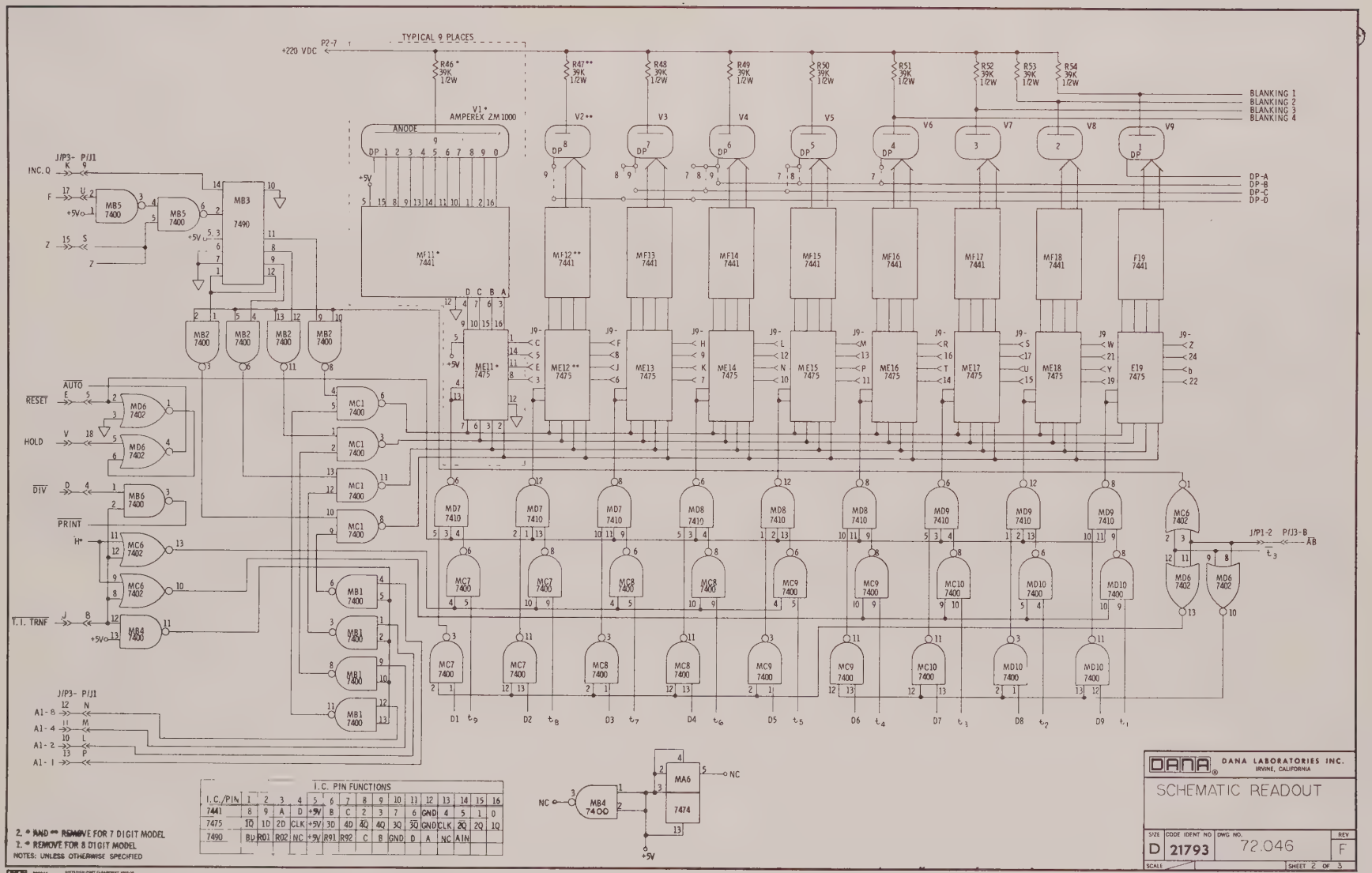
NOTES: UNLESS OTHERWISE SPECIFIED

DANA DANA LABORATORIES INC.
IRVINE, CALIFORNIA

SCHEMATIC READOUT

SIZE	CODE IDENT NO	DWG NO	REV
D	21793	721046	F

SCALE | SHEET 1 OF 3



I.C. PIN FUNCTIONS

I.C./PIN	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
7441	8	9	A	D	+5V	B	C	2	3	7	6	GND	4	5	1	0
7475	1Q	1D	2D	CLK	+5V	3Q	4D	4Q	4Q	3Q	3Q	GND	CLK	2Q	2Q	1Q
7490	BU	R01	R02	NC	+5V	R91	R92	C	B	GND	D	A	NC	AIN		

2. * AND ** REMOVE FOR 7 DIGIT MODEL
2. * REMOVE FOR 8 DIGIT MODEL
NOTES: UNLESS OTHERWISE SPECIFIED

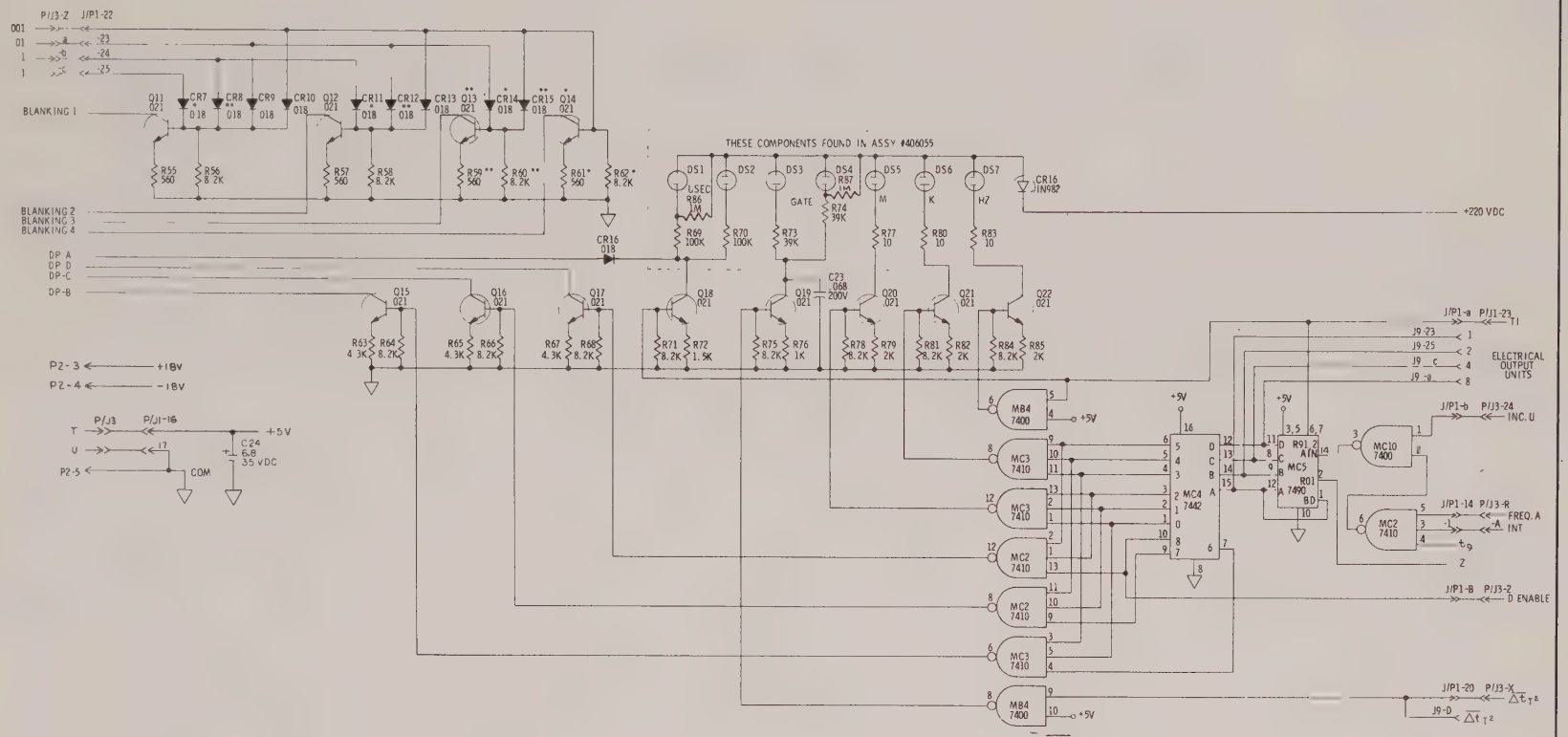
DANA DANA LABORATORIES INC.
IRVINE, CALIFORNIA

SCHEMATIC READOUT

SIZE	CODE IDENT NO	DWG NO.	REV
D	21793	72.046	F

SCALE

SHEET 2 OF 3



1. * DELETE ON 8 DIGIT MODEL,
* AND ** DELETE ON 7 DIGIT MODEL

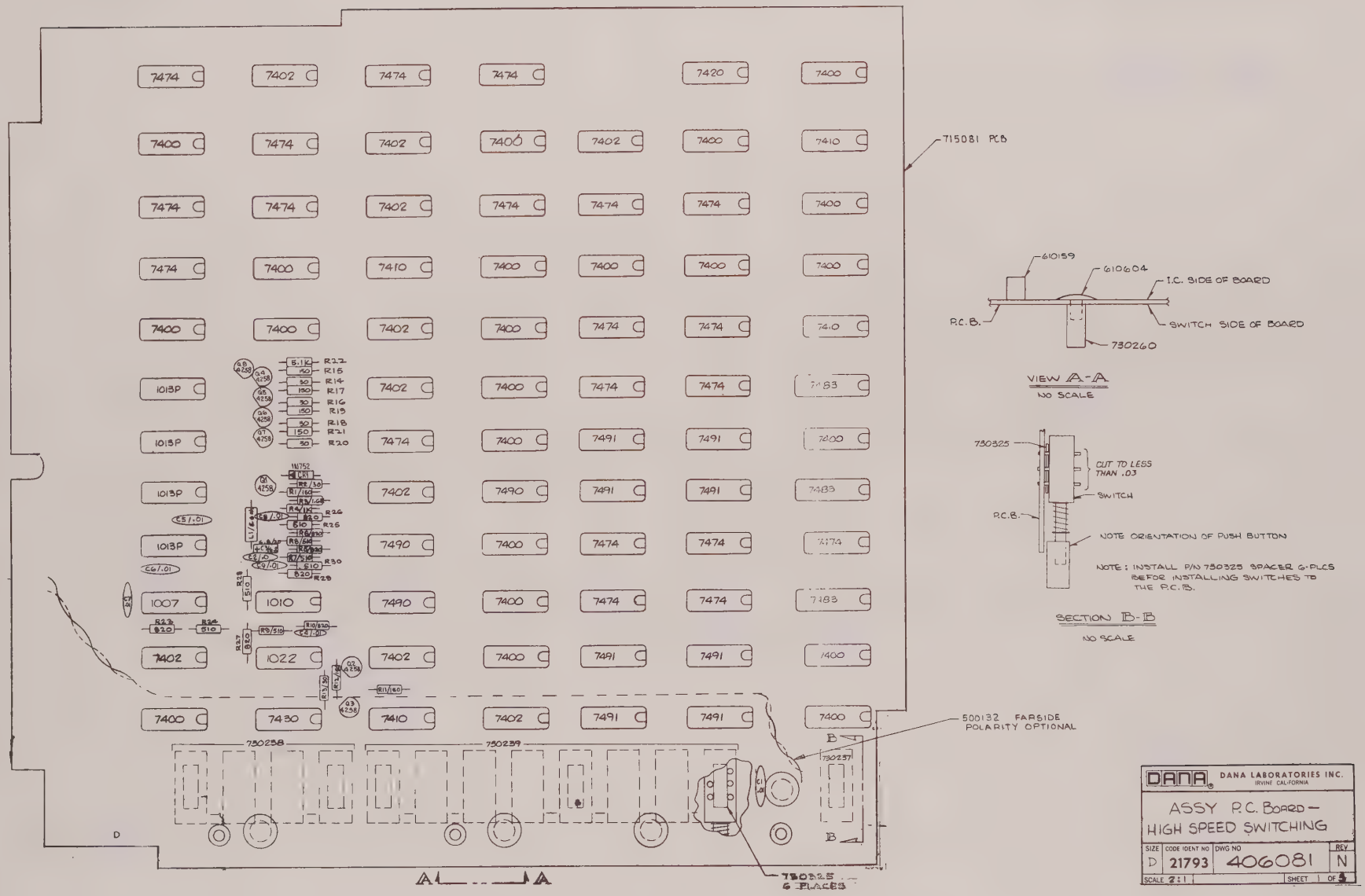
NOTES UNLESS OTHERWISE SPECIFIED

DANA LABORATORIES INC.
IRVINE CALIFORNIA

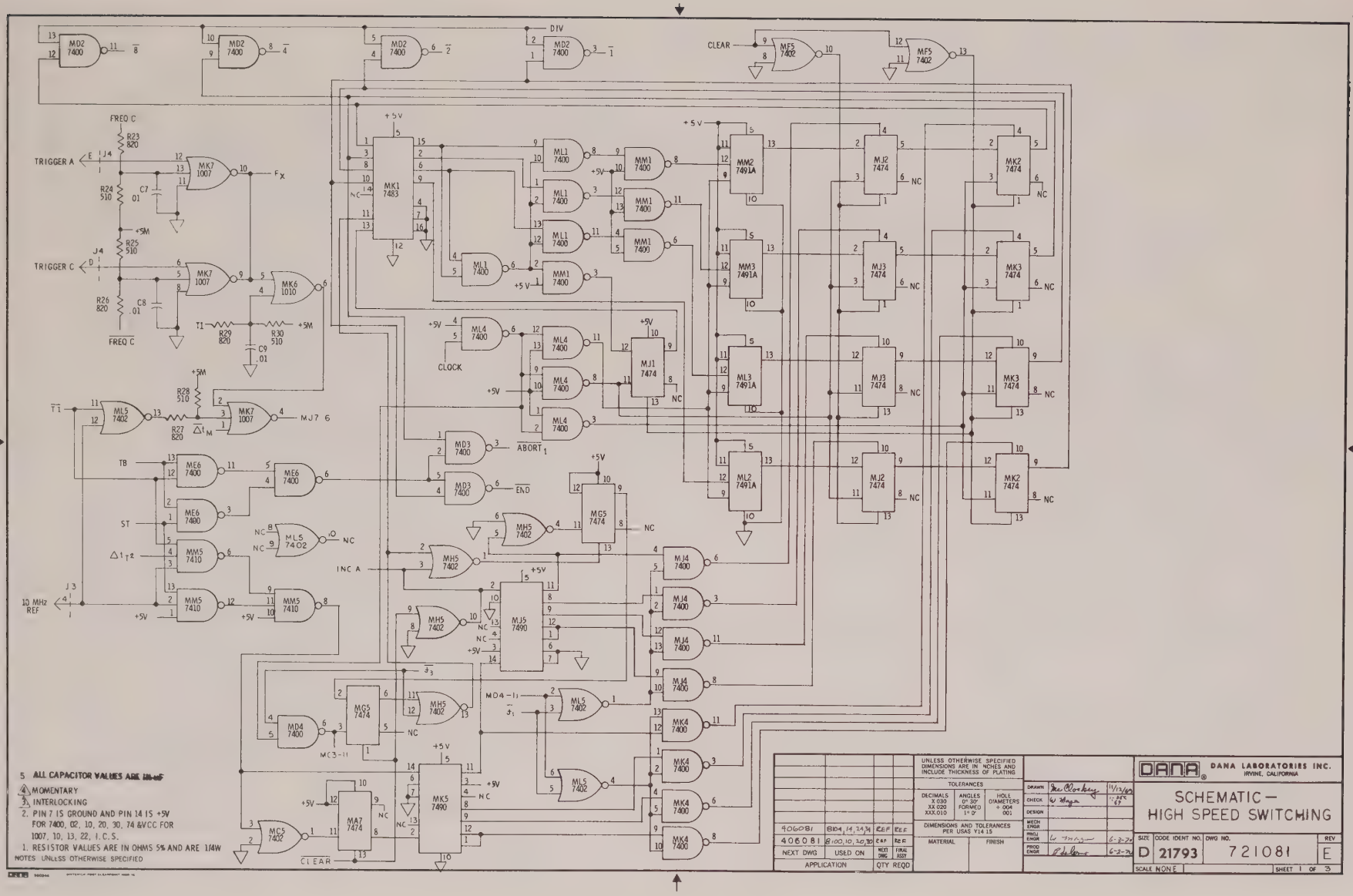
SCHEMATIC-READOUT

SIZE	CODE IDENT NO	DWG NO	REV
D	21793	721046	F

SCALE | SHEET 3 OF 3



DANA	DANA LABORATORIES INC. IRVINE CALIFORNIA
ASSY P.C. BOARD — HIGH SPEED SWITCHING	
SIZE: D	CODE IDENT NO: 21793
DWG NO: 406081	REV: N
SCALE 2:1	SHEET 1 OF 5



5 ALL CAPACITOR VALUES ARE IN uF

4 MOMENTARY

3 INTERLOCKING

2. PIN 7 IS GROUND AND PIN 14 IS +5V FOR 7400, 02, 10, 20, 30, 74 &VCC FOR 1007, 10, 13, 22, 1. C.S.

1. RESISTOR VALUES ARE IN OHMS 5% AND ARE 1/4W

NOTES UNLESS OTHERWISE SPECIFIED

406081	8104,14,34,74	EEF	EEF	
406081	8100,10,20,30,74	EEF	REF	
NEXT DWG	USED ON	NEXT DWG	FINAL ASSY	
APPLICATION		QTY REQD		

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE THICKNESS OF PLATING

TOLERANCES

DECIMALS	ANGLES	HOLE DIAMETERS
X .030	0° 30'	+ .004
XX .020	FORMED	- .001
XXX .010	1° 0'	

DIMENSIONS AND TOLERANCES PER USAS Y14.5

MATERIAL | FINISH

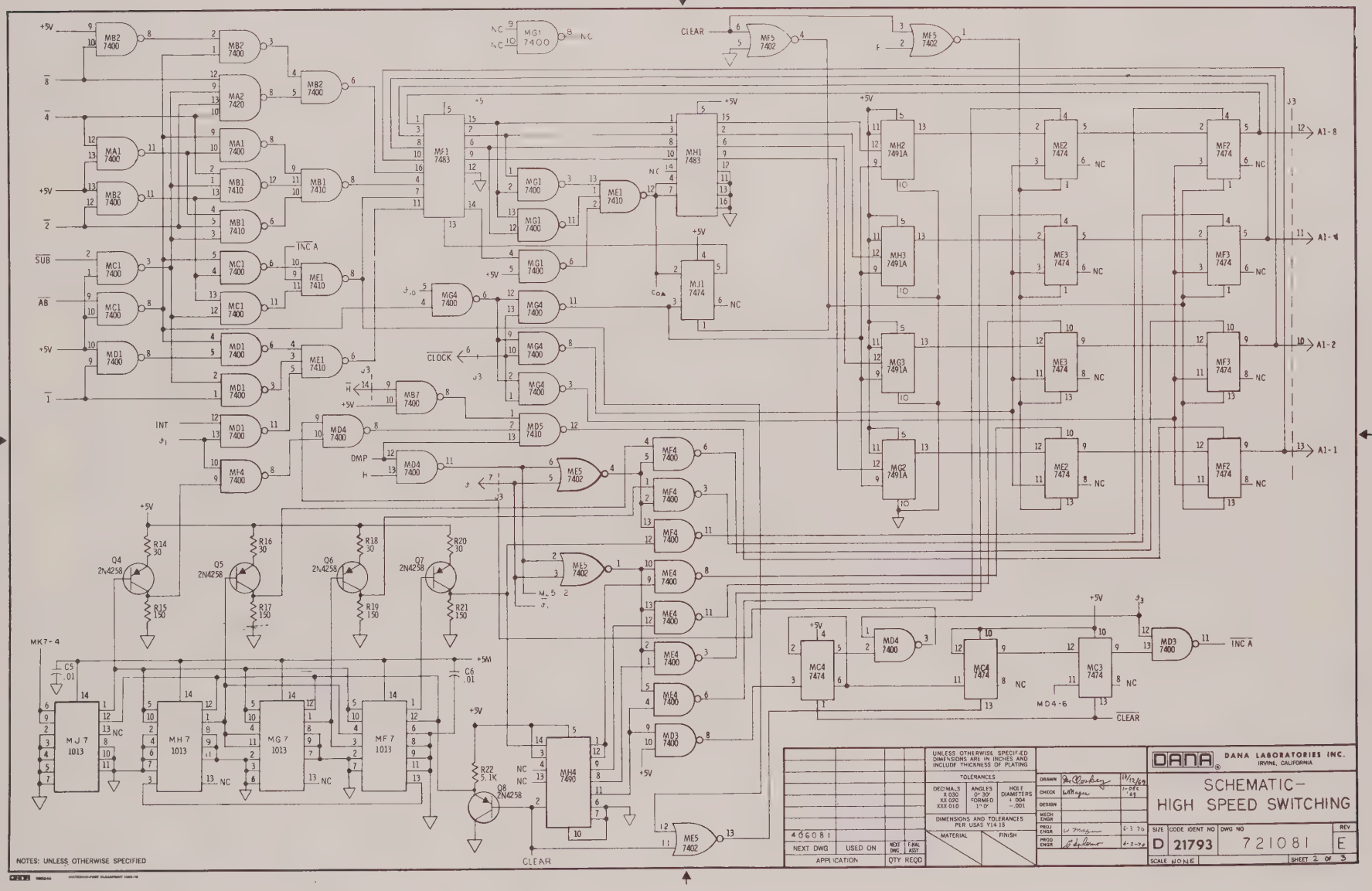
DRAWN	[illegible]	11/12/68
CHECK	[illegible]	11 DEC 68
DESIGN		
MECH ENGR		
PROJ ENGR	[illegible]	6-3-70
PROD ENGR	[illegible]	6-3-70

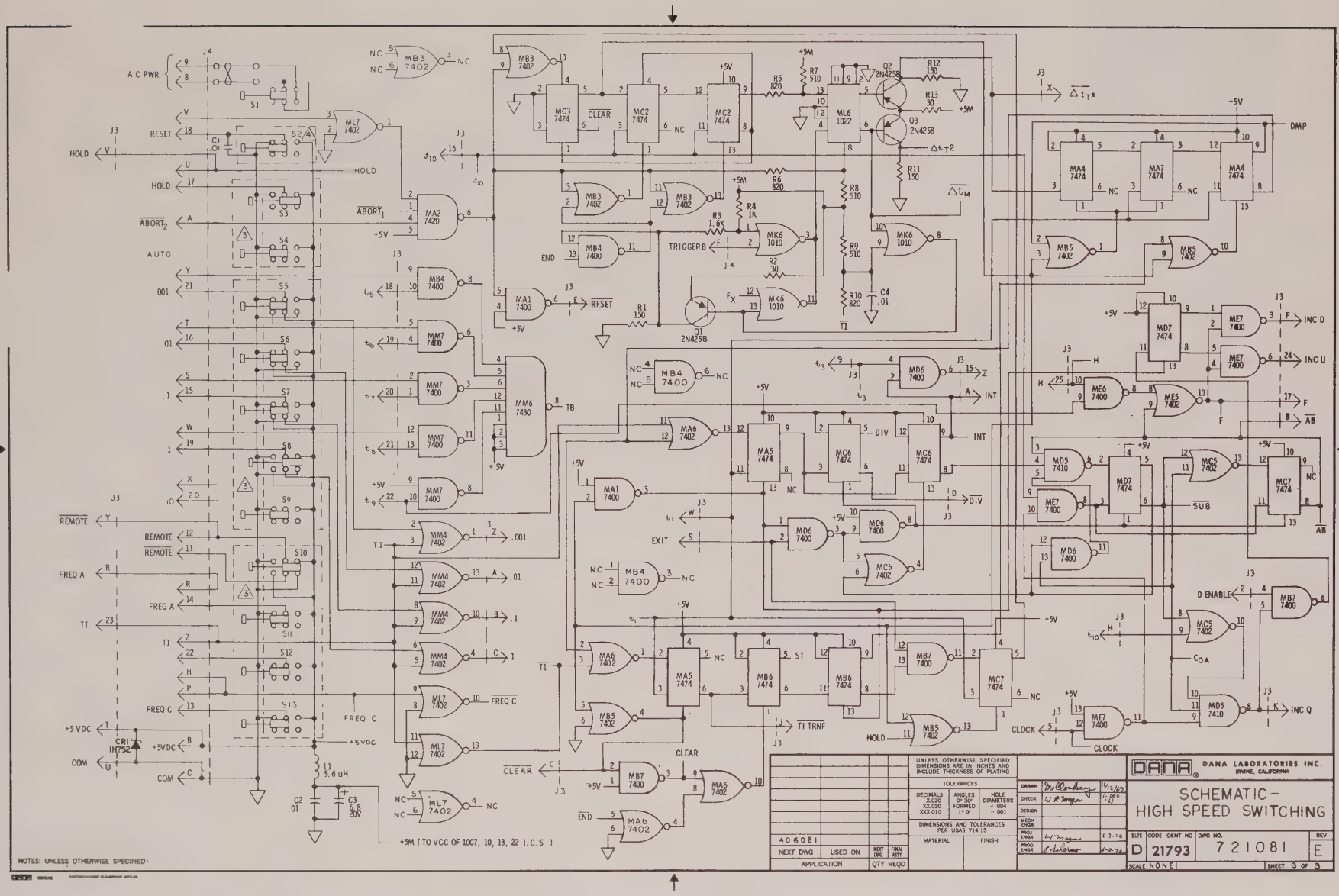
DANA DANA LABORATORIES INC. IRVINE, CALIFORNIA

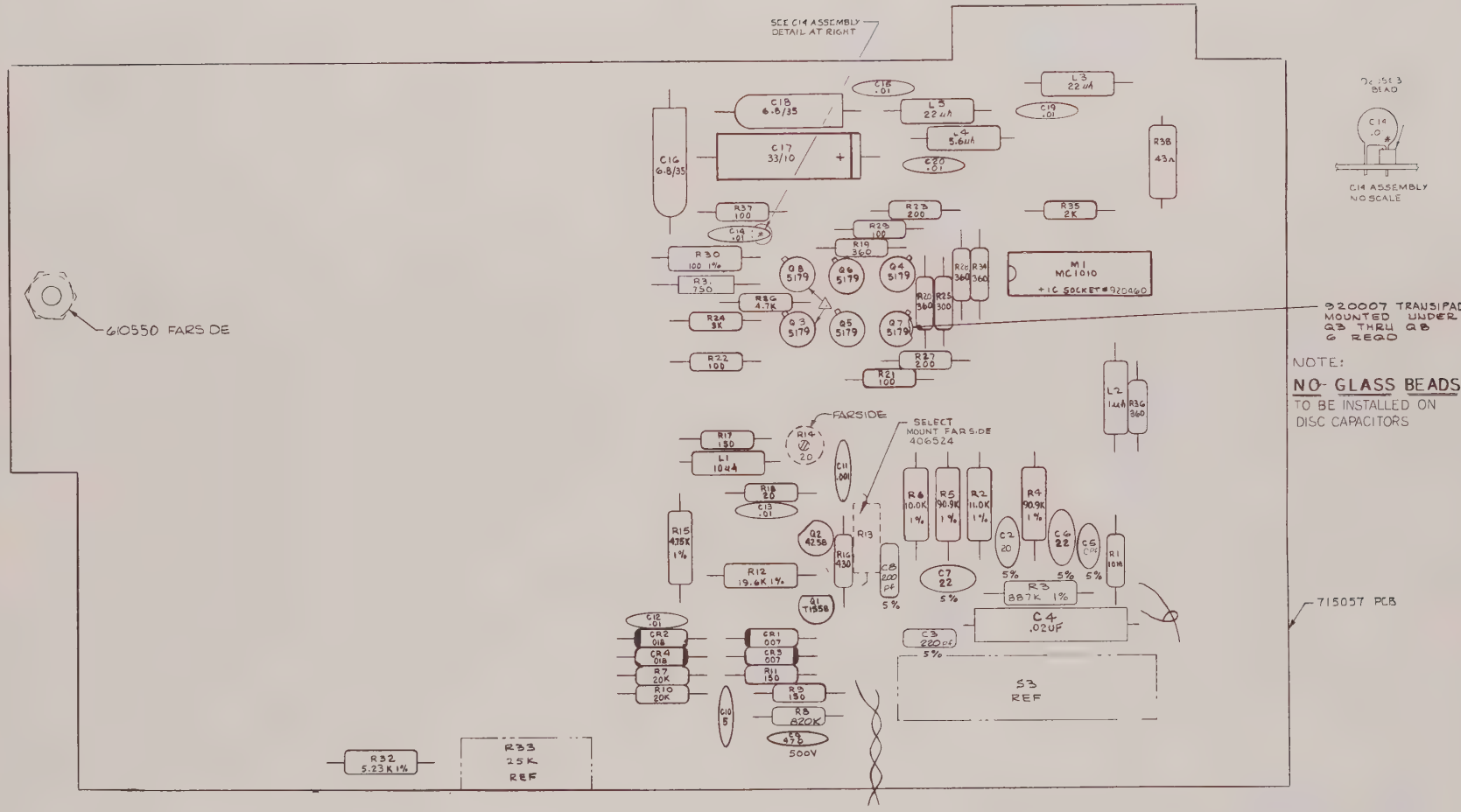
SCHEMATIC — HIGH SPEED SWITCHING

SIZE	CODE IDENT NO.	DWG NO.	REV
D	21793	721081	E

SCALE NONE | SHEET 1 OF 3


+5V
CLEAR
CLOCK
INT
DMP
INC A
SUB
AB
MK7-4
MD4-6
NOTES: UNLESS OTHERWISE SPECIFIED
CLEAR
A1-8
A1-4
A1-2
A1-1
INC A
CLEAR
DANA LABORATORIES INC.
IRVINE, CALIFORNIA
SCHEMATIC–
HIGH SPEED SWITCHING
SIZE D
CODE IDENT NO 21793
DWG NO 721081
REV E
SCALE NONE
SHEET 2 OF 3
406081
NEXT DWG
USED ON
APPLICATION
QTY REQD
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE THICKNESS OF PLATING
TOLERANCES
DECIMALS X .030 XX .020 XXX .010
ANGLES 0° 30' FORMED 1° 0'
HOLE DIAMETERS ± .004 –.001
DIMENSIONS AND TOLERANCES PER USAS Y14.15
MATERIAL
FINISH
DRAWN
CHECK
DESIGN
MECH ENGR
PROJ ENGR
PROD ENGR


A C PWR
RESET
HOLD
ABORT2
AUTO
.001
.01
.1
1
10
REMOTE
FREQ A
TI
FREQ C
+5 VDC
COM
CRI IN752
L1 5.6 uH
C2 .01
C3 6.8 20V
+5M (TO VCC OF 1007, 10, 13, 22 I.C.S)
ABORT1
RFSET
TRIGGER B
TB
EXIT
CLEAR
END
TI TRNF
INT
DIV
SUB
INC D
INC U
INC Q
D ENABLE
CLOCK
DMP
NOTES: UNLESS OTHERWISE SPECIFIED
DANA LABORATORIES INC.
IRVINE, CALIFORNIA
SCHEMATIC – HIGH SPEED SWITCHING
SIZE D
CODE IDENT NO 21793
DWG NO. 721081
REV E
SCALE NONE
SHEET 3 OF 3
406081
NEXT DWG
USED ON
APPLICATION
QTY REQD

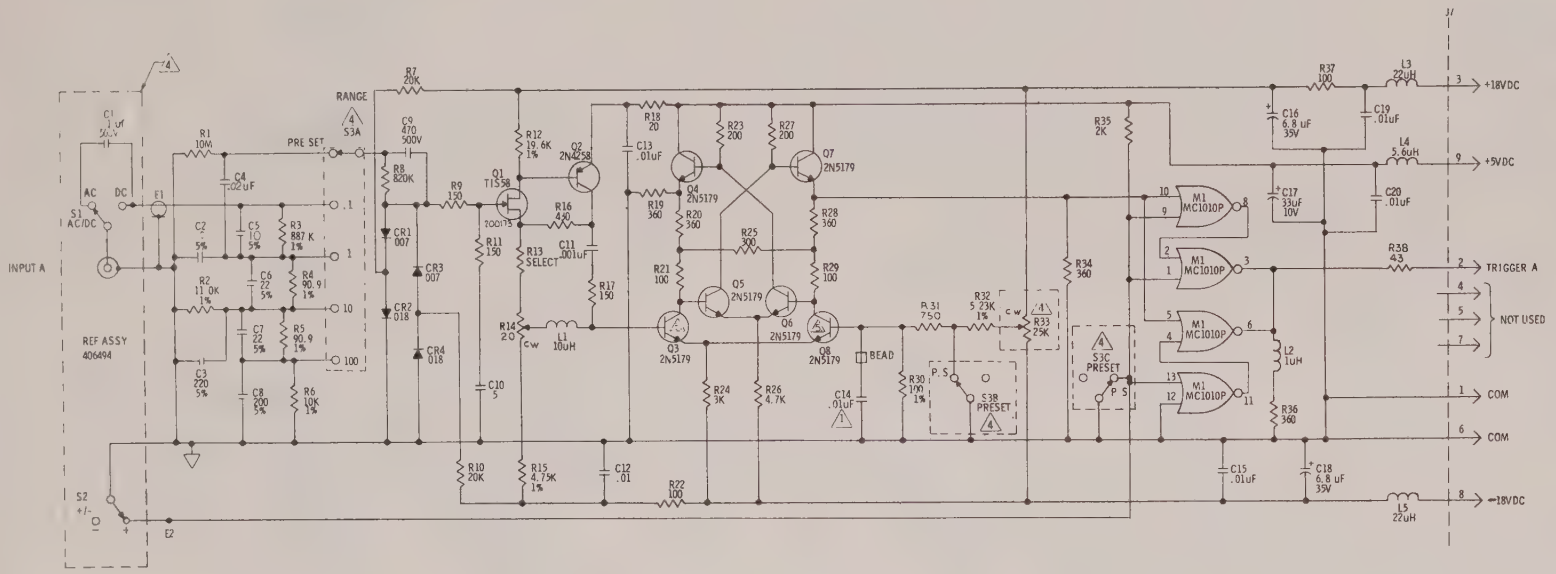


DANA DANA LABORATORIES INC. IRVINE CALIFORNIA

ASSY P.C. BOARD – 50 MHZ. PREAMP SINGLE

SIZE	CODE IDENT NO	DWG NO	REV
D	21793	406057	S

SCALE 4/1 SHEET 1 OF 4



3 Q3,Q8 IS MATCHED SET P/N 200186

4 PART OF ASSY NO. 406494

3. CAPACITOR VALUES ARE IN pF

2. RESISTOR VALUES ARE IN OHMS ± 5%

1 LEAD LENGTH TO BE 1/4 INCH FROM BASE OF Q8 TO C14

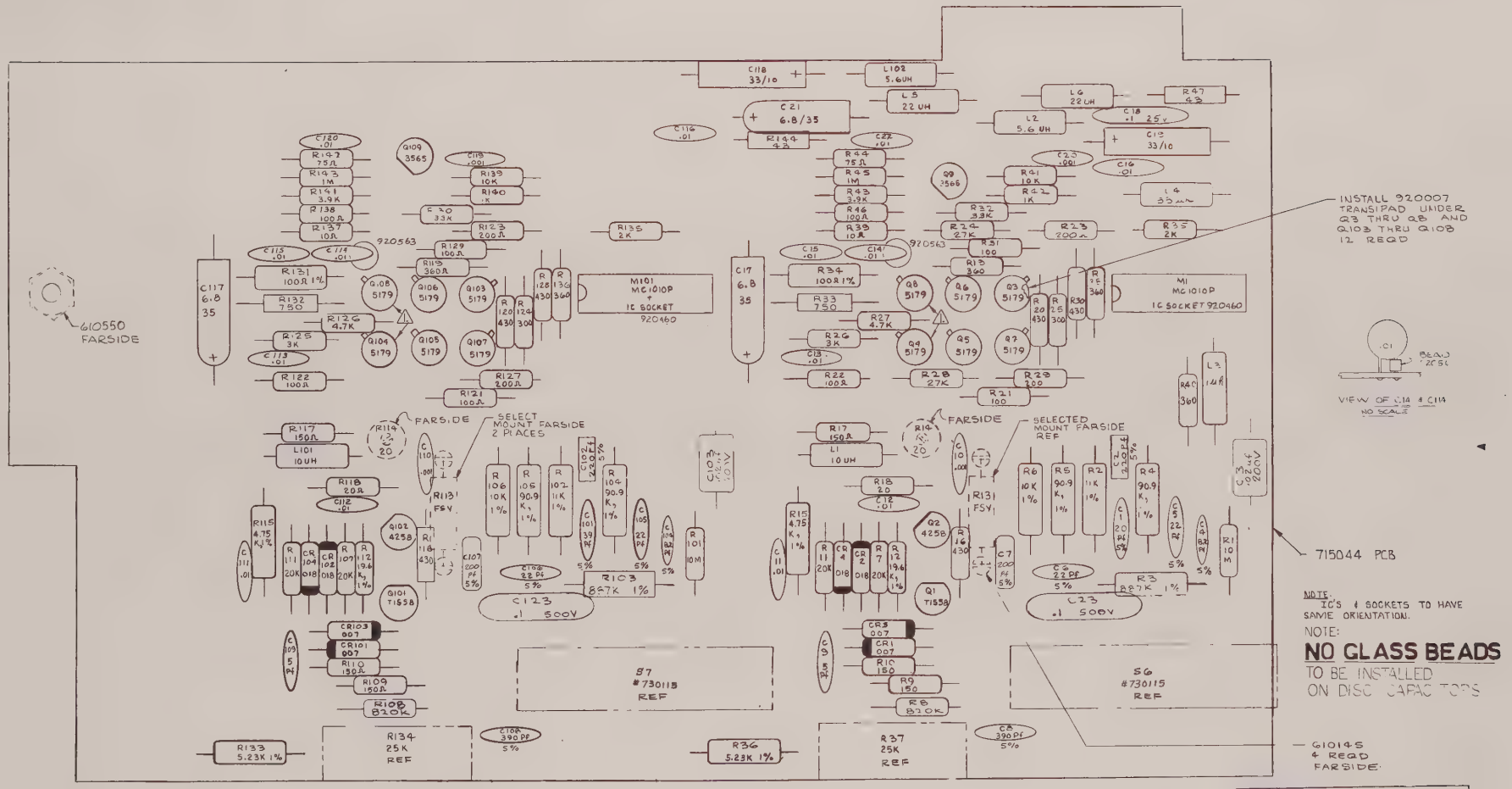
NOTES: UNLESS OTHERWISE SPECIFIED

DANA DANA LABORATORIES INC.
IRVINE, CALIFORNIA

SCHEMATIC —
50 MHz PREAMP
SINGLE CHANNEL

SIZE	CODE IDENT NO	DWG NO	REV
D	21793	721057	M

SCALE NONE | SHEET 1 OF 1



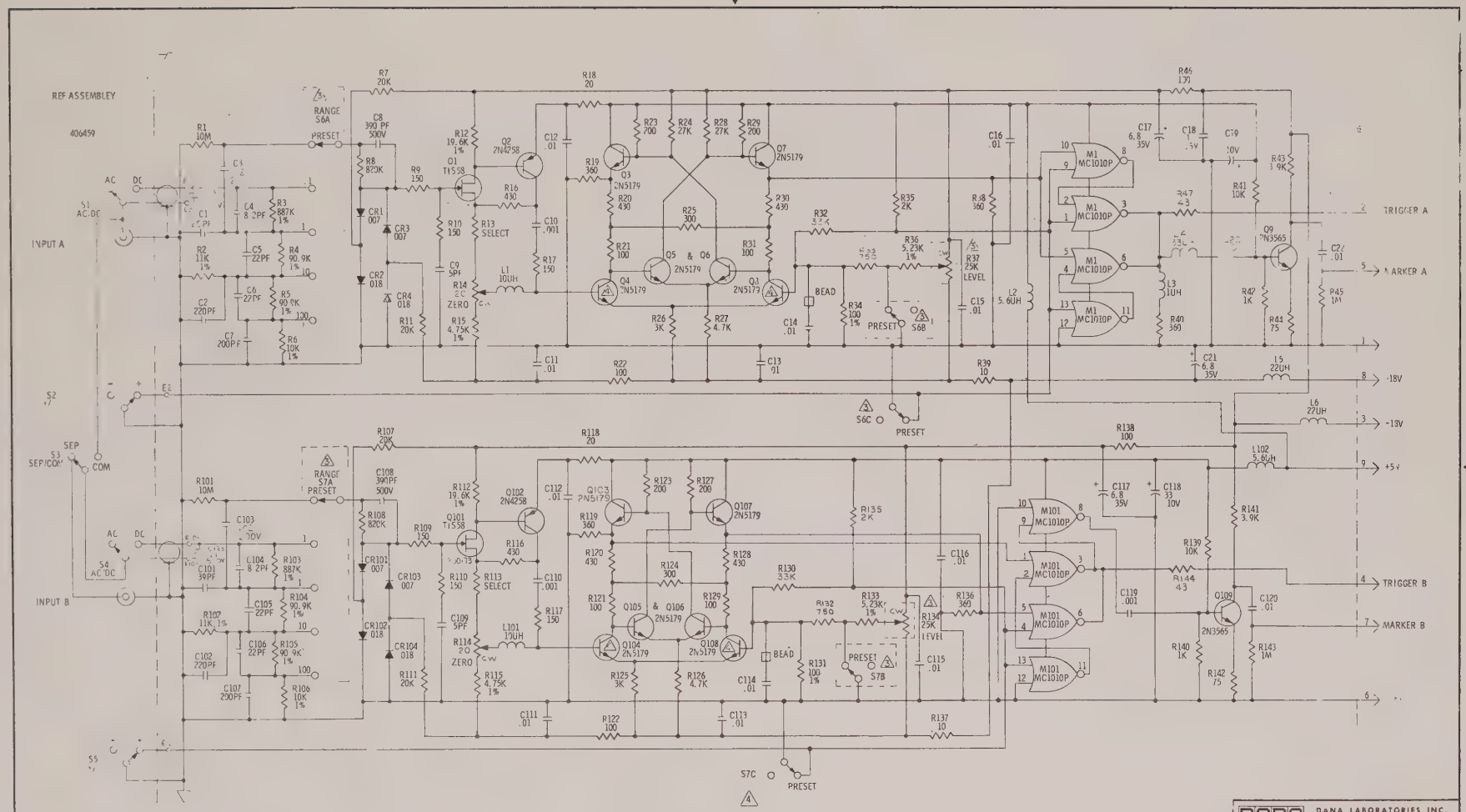
△ Q4 & Q8, Q104 & Q105 ARE MATCHED SETS PN 200106

DANA DANA LABORATORIES INC

ASSY P.C. BOARD - 50 MHZ PREAMP DUAL

SIZE	CODE IDENT NO	DWG NO	REV
D	21793	406044	S

SCALE 4/1 SHEET 1 OF 2



LAST DESIGNATORS

R	C	Q	CR	L	M	S
147	123	9	4	6	1	7
144	123	103	104	102	101	7C

NOTES UNLESS OTHERWISE SPECIFIED

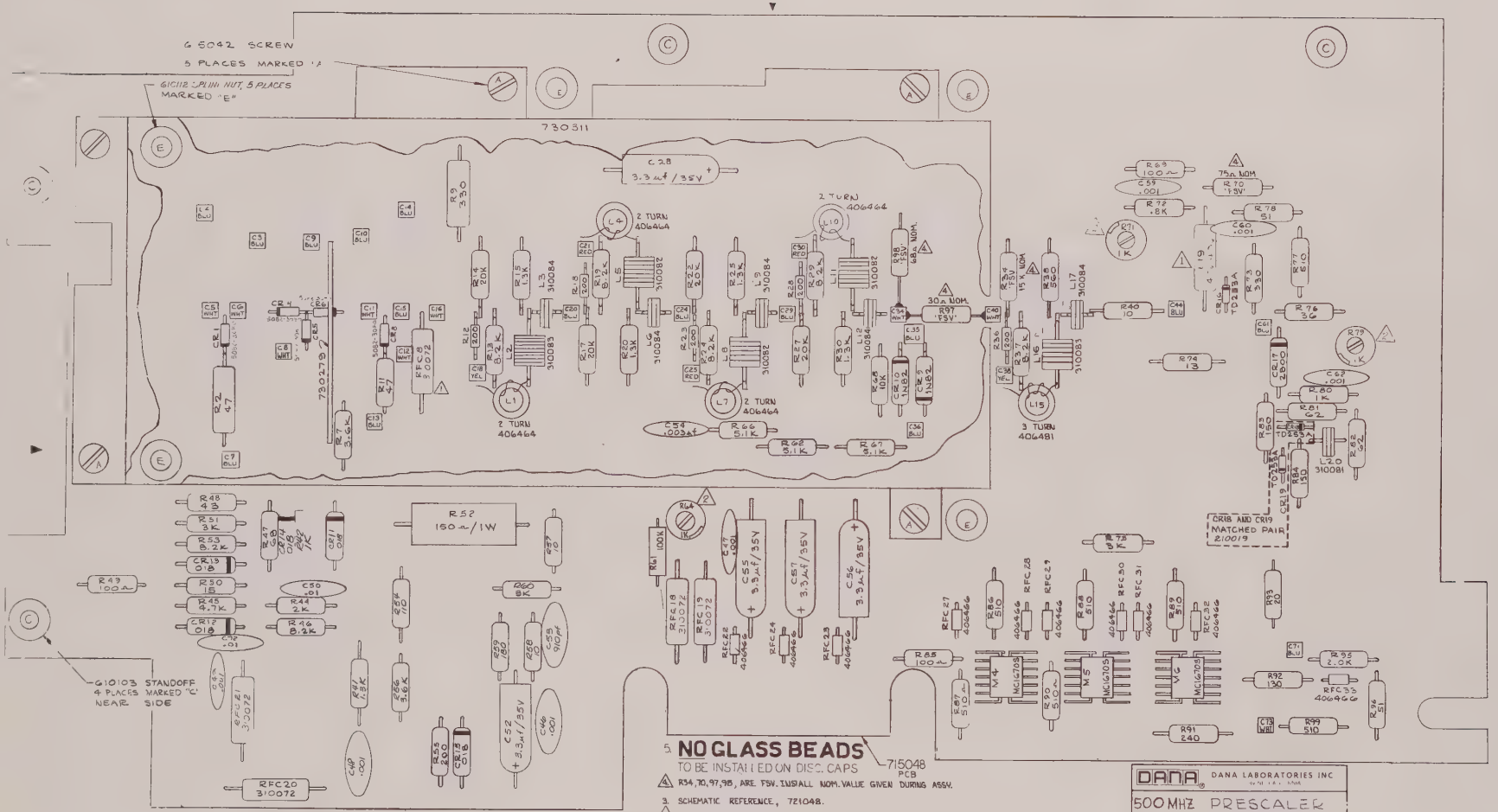
1. PART OF ASSY. NO. 406459.
2. CAPACITOR VALUES ARE IN UF + 10% 100V.

DANA LABORATORIES INC.
IRVINE CALIFORNIA

SCHEMATIC
50 MHZ

SIZE	COORD IDENT NO	DWG NO	REV
D	21793		L

SCALE | SHEET OF



5. **NO GLASS BEADS** TO BE INSTALLED ON DISC. CAPS — 715048 PCB

4. R34, 70, 97, 98, ARE FSV. INSTALL NOM. VALUE GIVEN DURING ASSY.

3. SCHEMATIC REFERENCE, 721048.

2. AFTER FINAL TEST APPLY PAINT-TORQUE P/N 980430 TO POTS R64, R71 & R79

1. INSTALL CASE APPROX. 1/16" ABOVE BOARD

NOTE: UNLESS OTHERWISE SPECIFIED

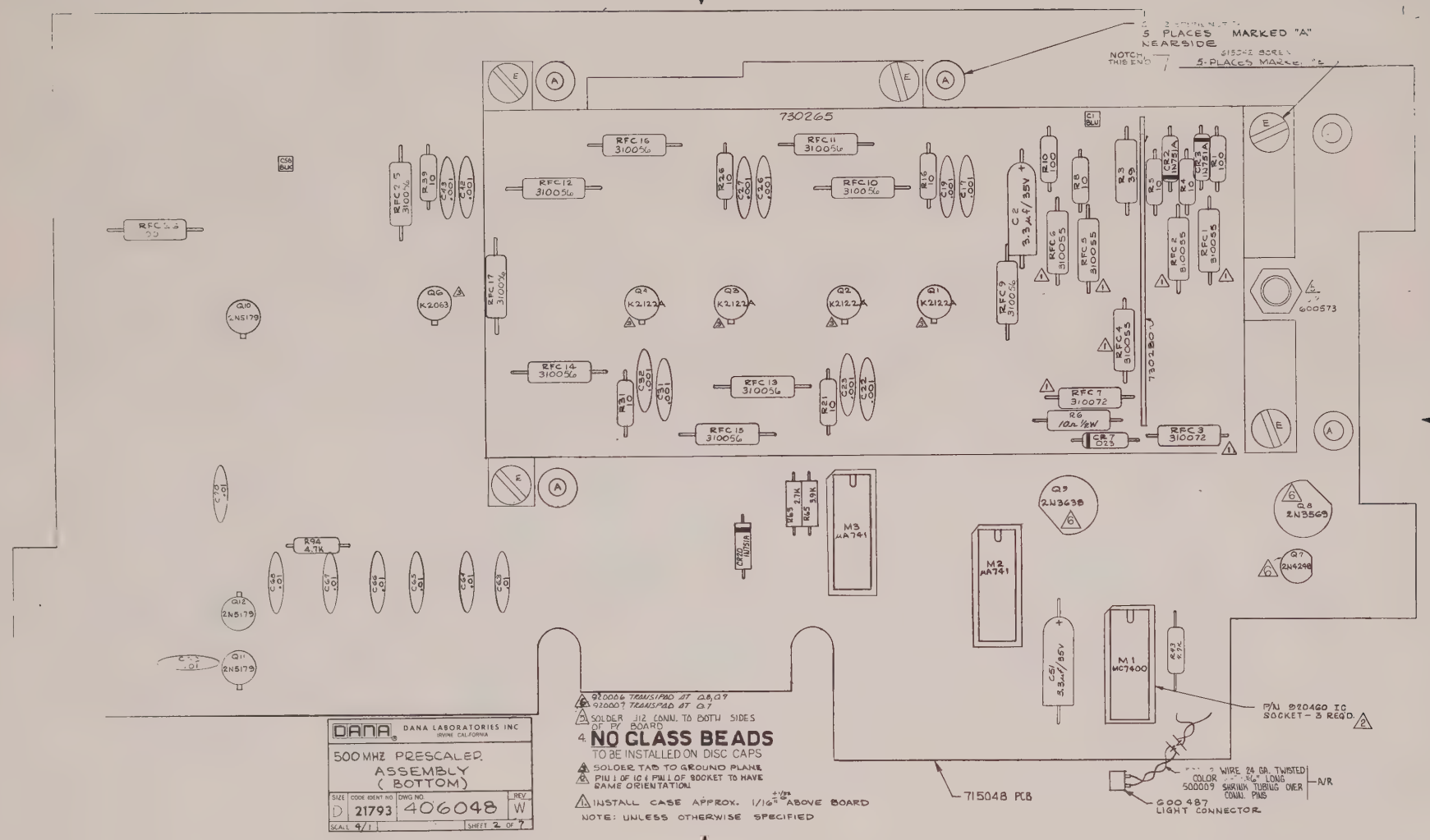
DANA LABORATORIES INC

500 MHZ PRESCALER ASSEMBLY (TOP)

SZE	CODE IDENT NO	DWG NO	REV
D	21793	406048	W

SCALE 4/1 SHEET 1 OF 7

REL PER DRN 968 June 5 70



DANA DANA LABORATORIES INC IRVINE CALIFORNIA

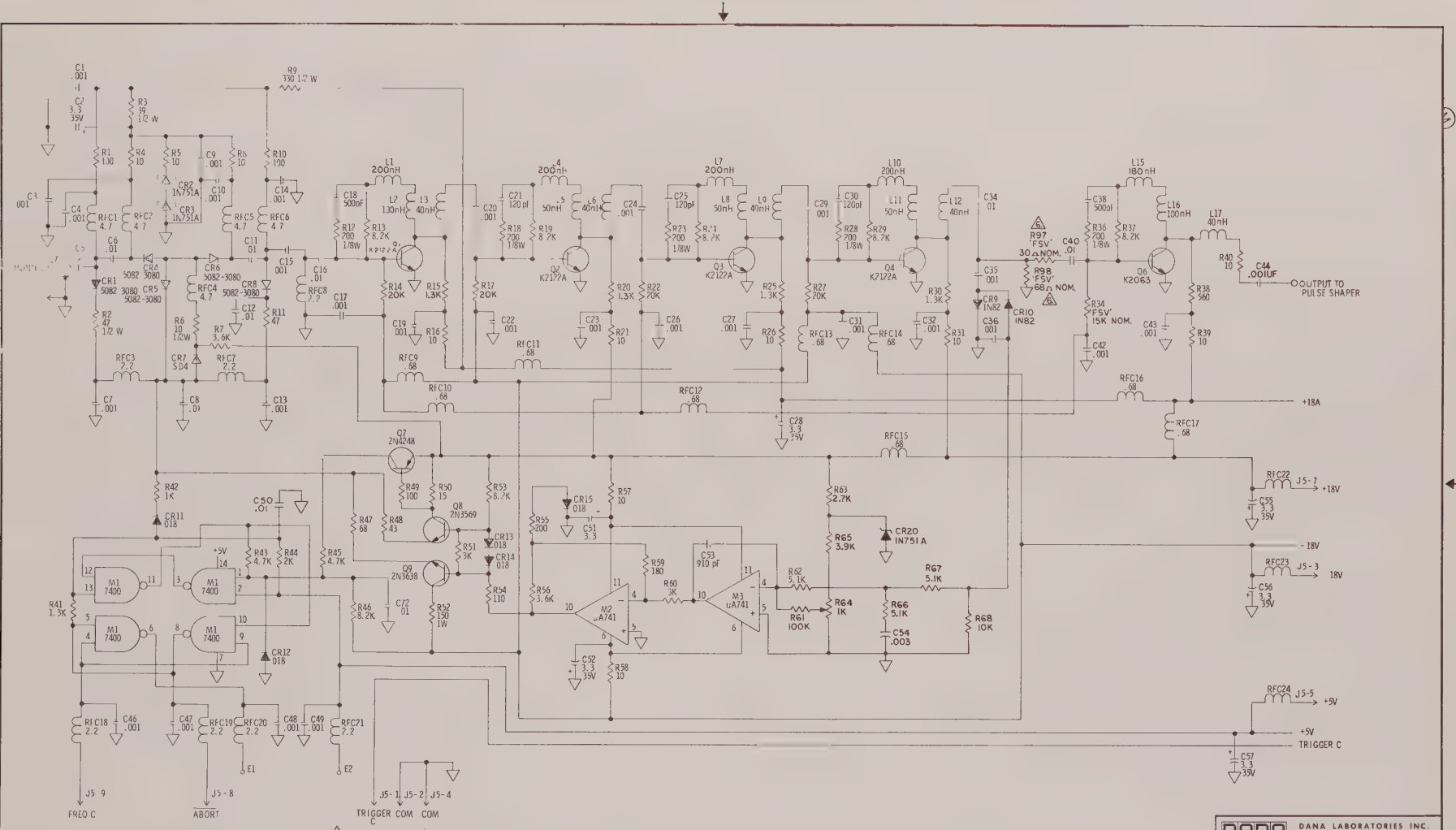
500 MHZ PRESCALER ASSEMBLY (BOTTOM)

SIZE	CODE IDENT NO	DWG NO	REV
D	21793	406048	W

SCALE 4/1 SHEET 2 OF 7

1. 920006 TRANSPAD AT Q8, Q9
2. 920007 TRANSPAD AT Q7
3. SOLDER .312 CONN. TO BOTH SIDES OF PC BOARD
4. **NO GLASS BEADS** TO BE INSTALLED ON DISC CAPS
5. SOLDER TAB TO GROUND PLANE
6. PIN 1 OF IC & PIN 1 OF SOCKET TO HAVE SAME ORIENTATION
7. INSTALL CASE APPROX. $1/16^{\pm 1/32}$" ABOVE BOARD

NOTE: UNLESS OTHERWISE SPECIFIED



△6 VALUES FOR R97 & R98 ARE CALCULATED FROM THE FOLLOWING FORMULAE: $\frac{R1 \cdot (R2+30)}{R1+R2+30} = 30 \pm 15\%$

5. ALL CAPACITOR VALUES ARE IN uF
4. ALL CHIP CAPACITORS ARE COLOR CODED AS FOLLOWS,

10 pf	(100039)	BLACK
120 pf	(350312)	RED
900 pf	(350137)	YELLOW
.001 uf	(350136)	BLUE
.01 uf	(350138)	WHITE

2. ALL CHOKE VALUES ARE IN uH
1. ALL RESISTORS VALUES ARE IN OHMS AND ARE 1/4W, 5%

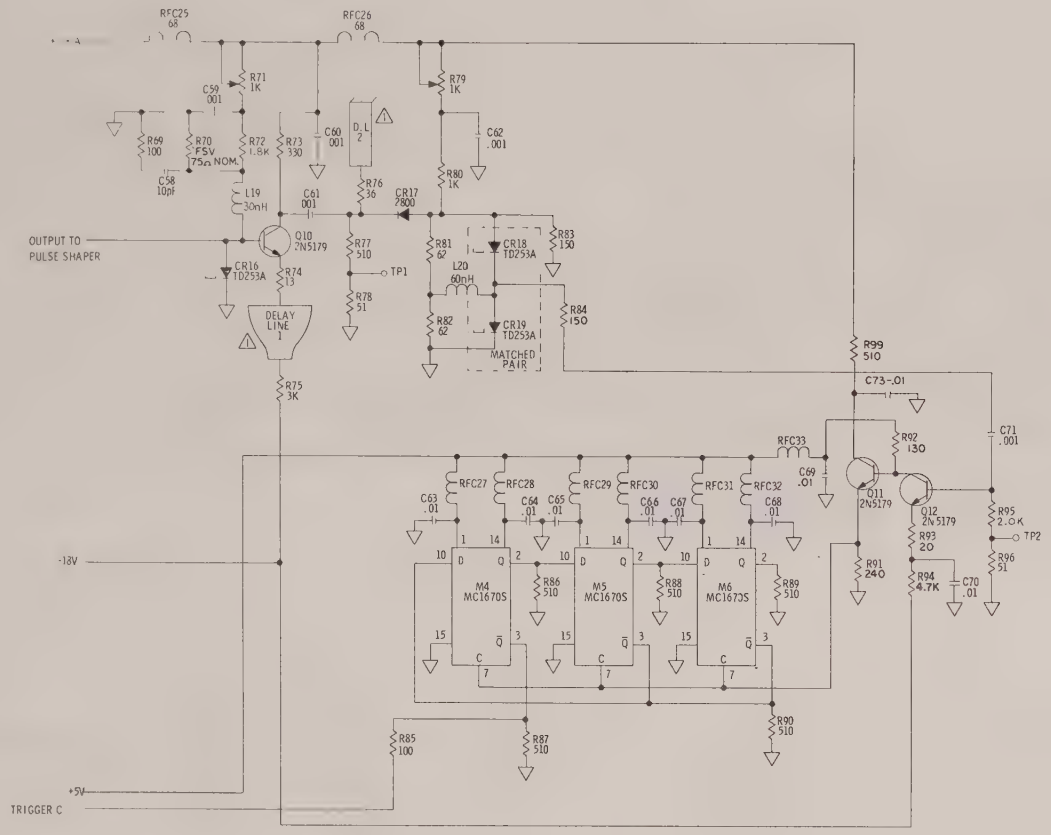
NOTES: UNLESS OTHERWISE SPECIFIED

DANA DANA LABORATORIES INC.
IRVINE, CALIFORNIA

SCHEMATIC
500 MHz PRESCALER

SIZE	CODE IDENT NO	DWG NO	REV
D	21793	721048	L

SCALE | SHEET 1 OF 2



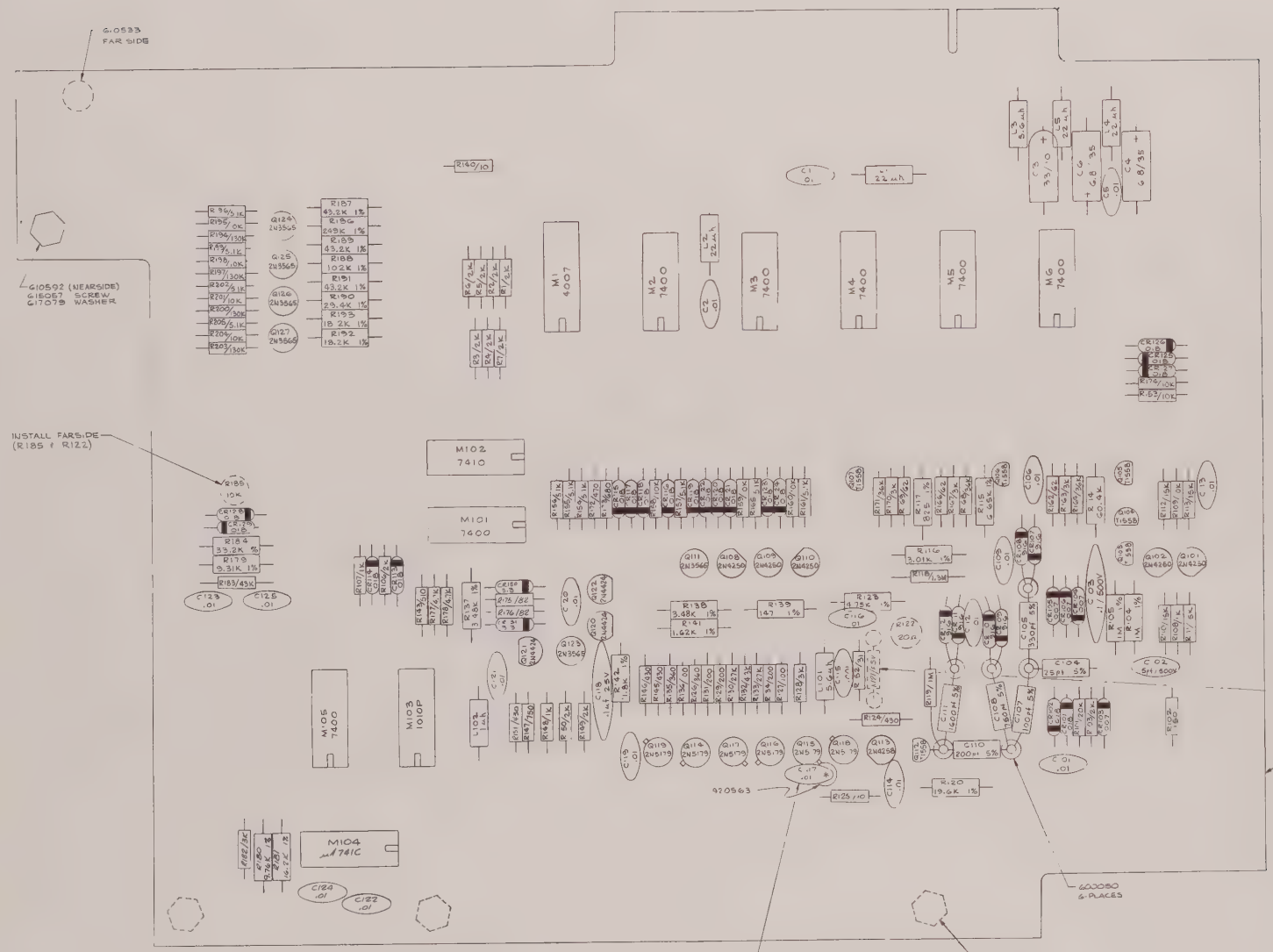
⚠ NOTE ETCHED ON P.C. BOARD
NOTES UNLESS OTHERWISE SPECIFIED

DANA LABORATORIES INC.
IRVINE, CALIFORNIA

SCHEMATIC
500 MHz PRESCALER

SIZE	CODE IDENT NO	DWG NO	REV
D	21793	721048	L

SCALE | SHEET 2 OF 2



NOTE:
DO NOT INSTALL GLASS BEADS
ON DISC CAPACITORS.

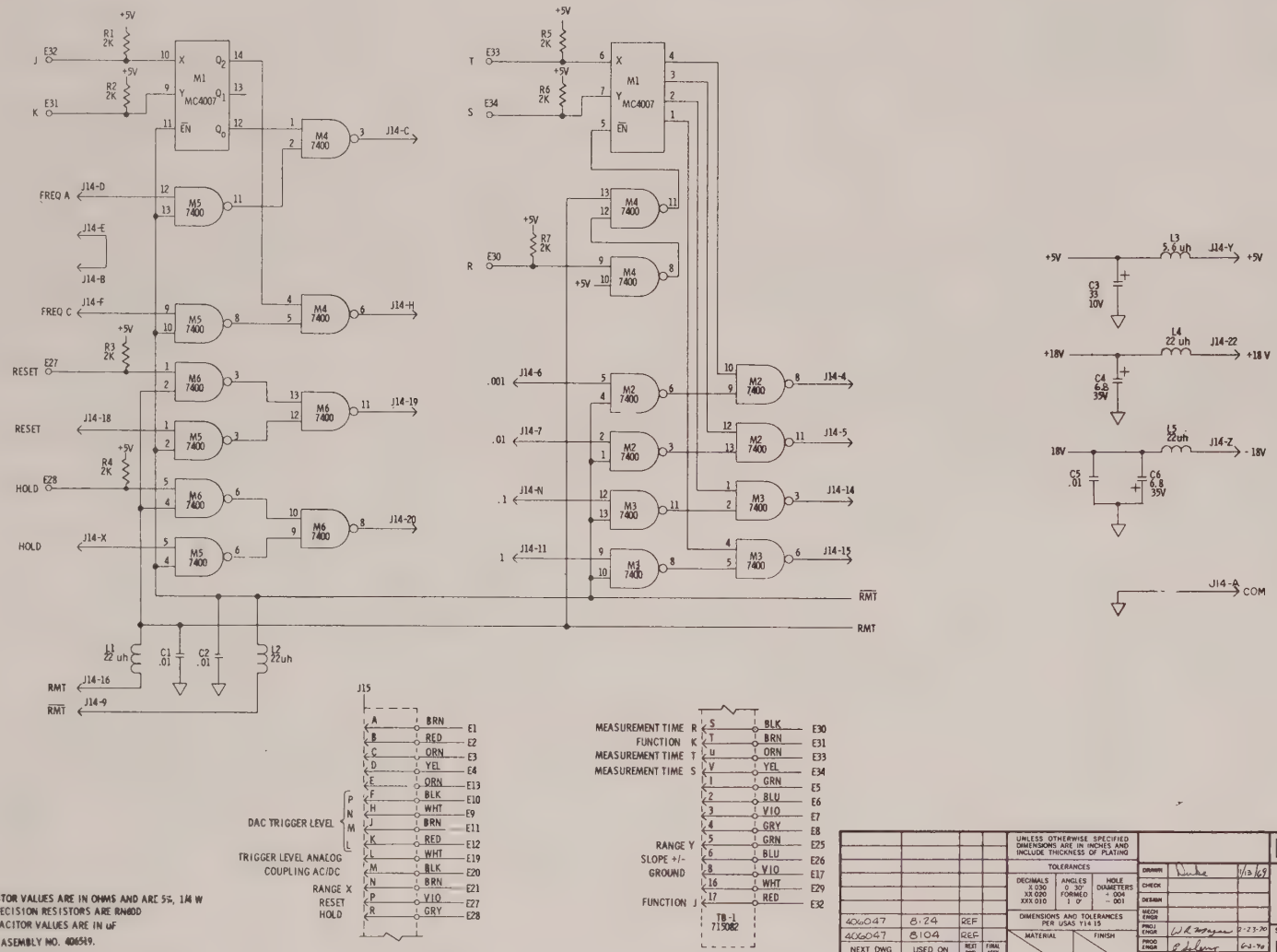
NOTES:
1. ALL I.C. HAVE SOCKETS

DWG NO	REV
406047	M
SHEET	OF 6

DANA DANA LABORATORIES INC
IRVINE, CALIFORNIA

ASSY: P.C.B.
PROGRAM SIGNAL COND.
SINGLE

SIZE	CODE IDENT NO	DWG NO	REV
R	21793	406047	M
SCALE 4:1		SHEET 1 OF 6	



4. ALL RESISTOR VALUES ARE IN OHMS AND ARE 5%, 1/4 W
5. ALL 1% PRECISION RESISTORS ARE RN60D
2. ALL CAPACITOR VALUES ARE IN uF

⚠ PART OF ASEMBLY NO. 406549.

NOTES: UNLESS OTHERWISE SPECIFIED

406047	8.24	REF	
406047	8104	REF	
NEXT DWG	USED ON	REQT DWG	FINAL ASSY
APPLICATION		QTY REQD	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE THICKNESS OF PLATING

TOLERANCES

DECIMALS	ANGLES	HOLE DIAMETERS
X .030	0 30'	- .004
XX .020	FORMED	- .001
XXX .010	1 0°	

DIMENSIONS AND TOLERANCES PER USAS Y14.15

MATERIAL | FINISH

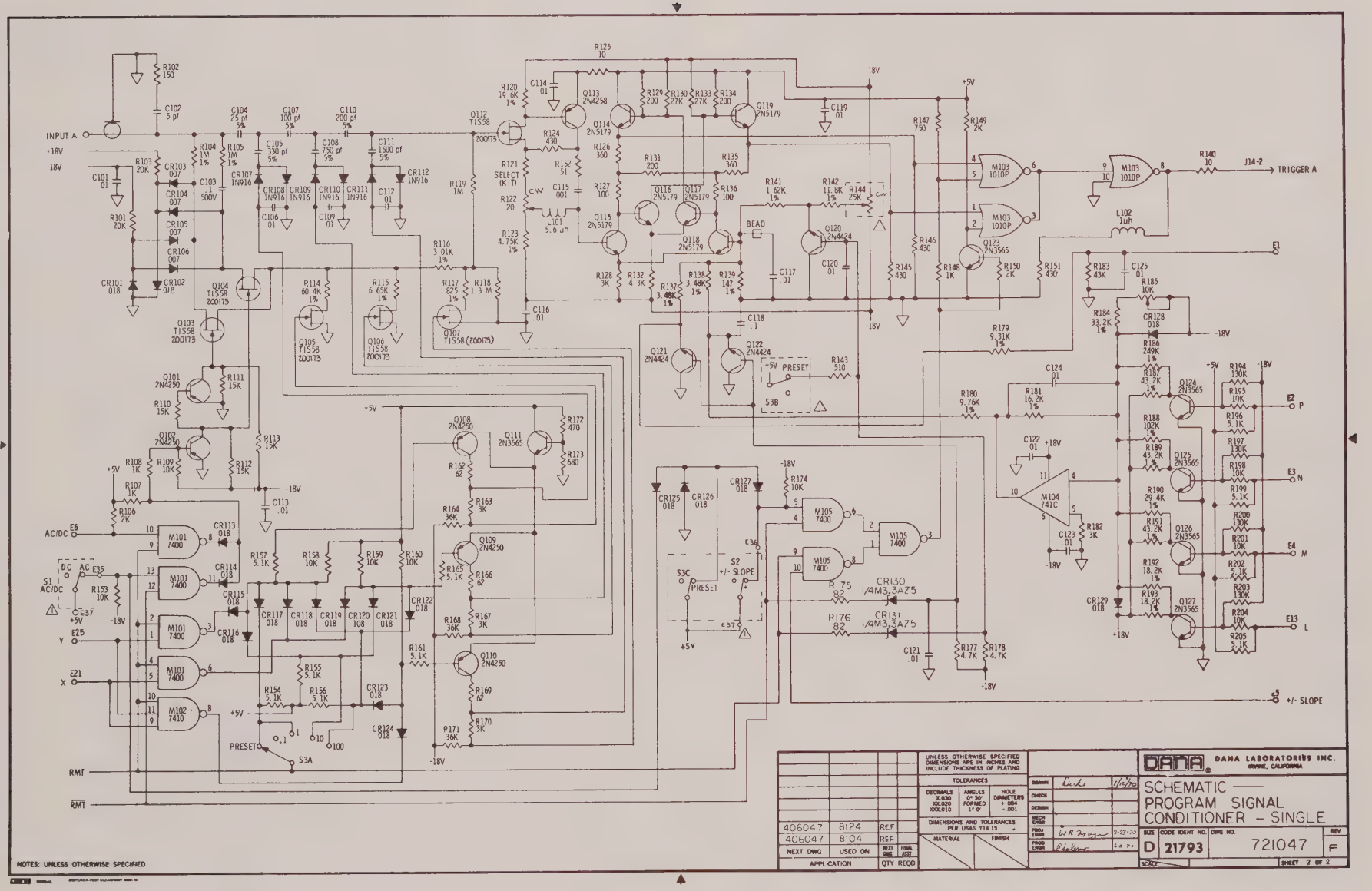
DRAWN	Rinke	11/12/69
CHECK		
DESIGN		
MECH ENGR		
PROJ ENGR	W.R. Morgan	2-23-70
PROD ENGR	Edelman	6-1-70

DANA DANA LABORATORIES INC. IRVINE, CALIFORNIA

SCHEMATIC PROGRAM SIGNAL CONDITIONER - SINGLE

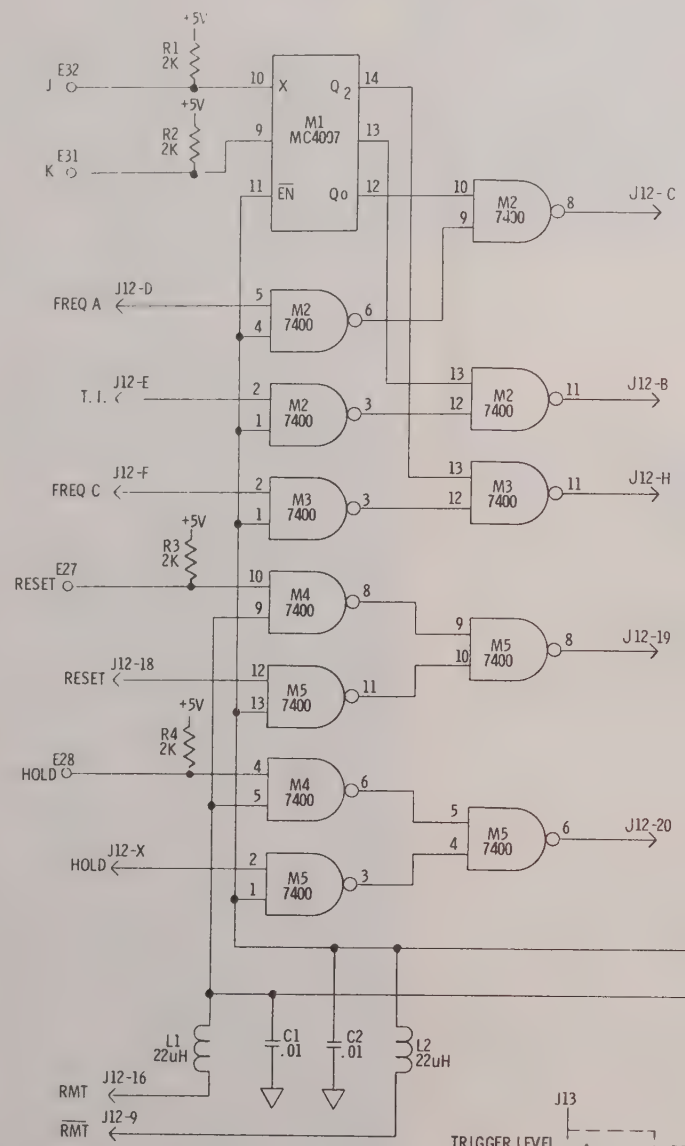
SIZE	CODE IDENT NO.	DWG NO.	REV
D	21793	721047	F

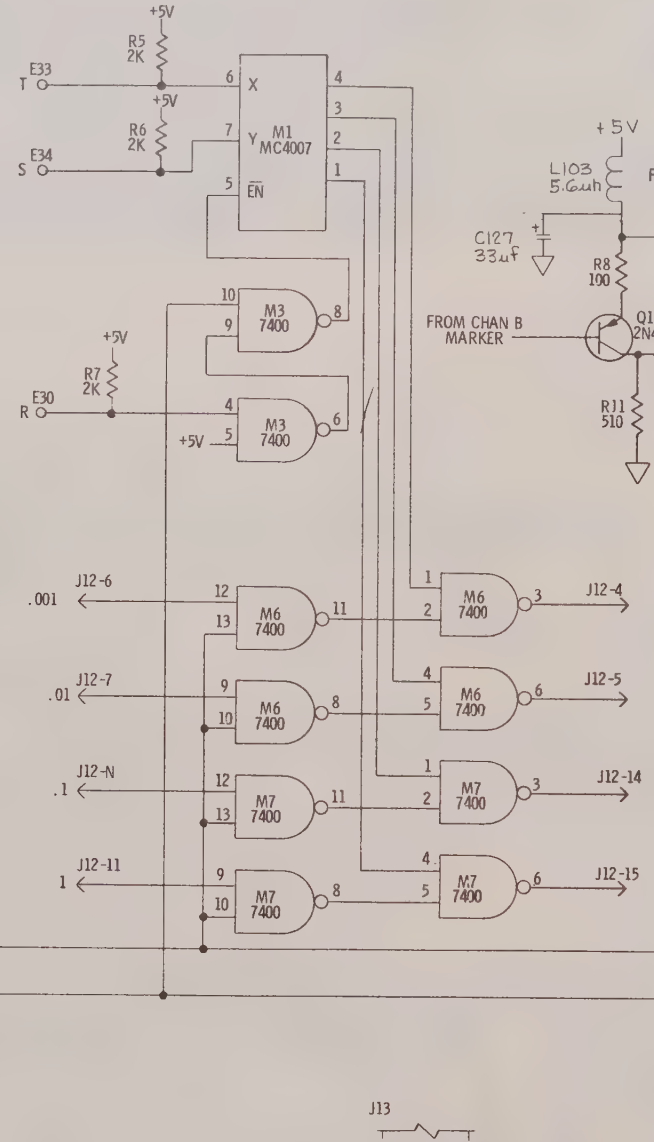
SCALE | SHEET 1 OF 2

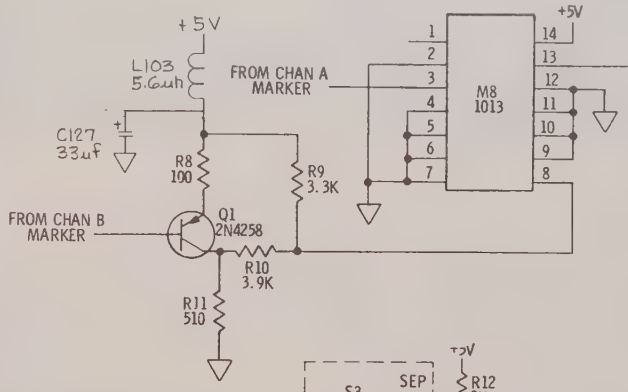

INPUT A
+18V
-18V
AC/DC
RMT
PRESET
TRIGGER A
+/- SLOPE
BEAD
PRESET
+/- SLOPE
DANA LABORATORIES INC.
IRVINE, CALIFORNIA
SCHEMATIC — PROGRAM SIGNAL CONDITIONER - SINGLE
D 21793 721047 F
SHEET 2 OF 2
406047 8124 REF
406047 8104 REF
NEXT DWG USED ON
APPLICATION QTY REQD
NOTES: UNLESS OTHERWISE SPECIFIED

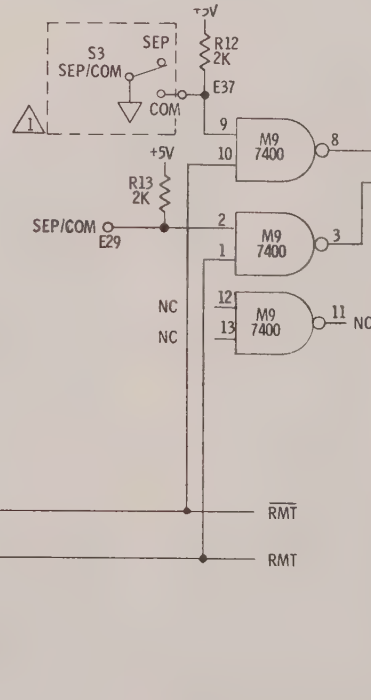
REVISIONS				
LTR	DESCRIPTION	DR	CHK	APP'D
J	REVISE PER E.O. 6395	CARROLL 3-4		
K	REVISED PER EO 6389	DRAWN 21 NOV 71		
L	REVISED PER EO-7463	DRAWN 10 MAY 72		
M	REVISED PER EO 7650	JE 12-72		
N	CHANGE R140, 340, 1028 & 3028 EO 8035	JE 3/8/73		
P	REVISED-EO 8151	JE 6-73		

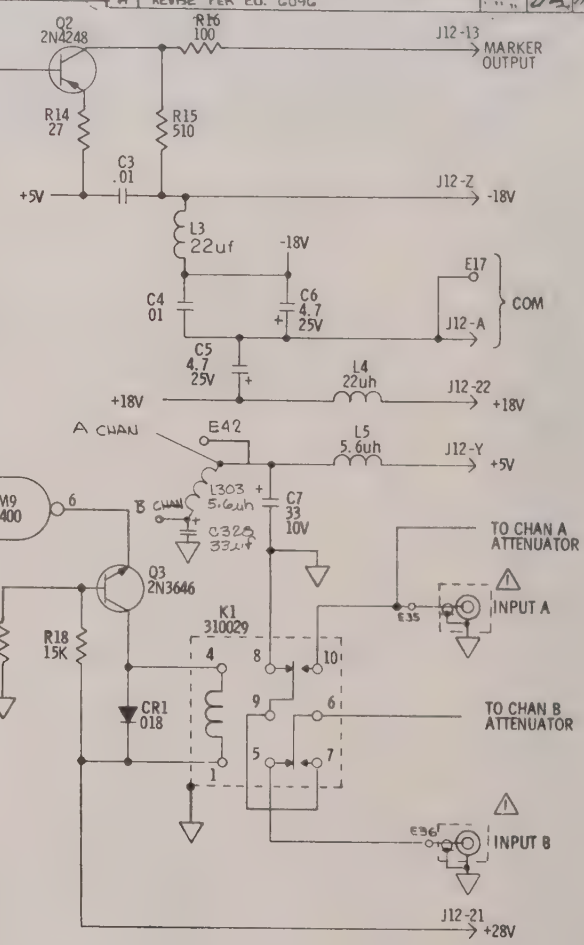
REVISIONS				
LTR	DESCRIPTION	DR	CHK	APP'D
D	RELEASED PER ~~DRN~~ REV "C"			
E	INCORP S.C. 703, 715, 792,			
F	INCORP SC 807			
G	INCORP SC 822			
H	REL PER DRN 983			
	REVISE PER EO. 6096			

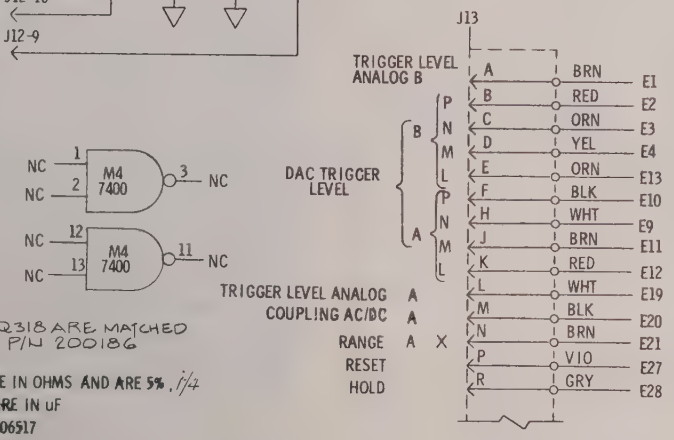


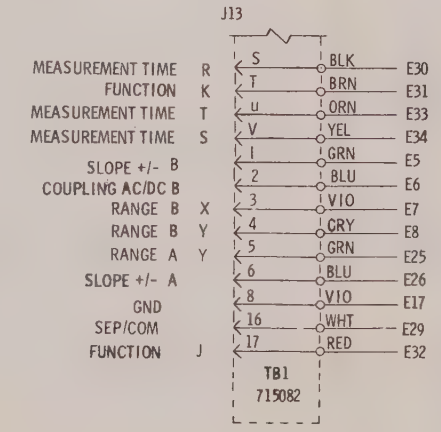












4 Q115 & Q113, Q315 & Q318 ARE MATCHED PAIR PER DANA P/N 200186

3. ALL RESISTOR VALUES ARE IN OHMS AND ARE 5%, 1/4
2. ALL CAPACITOR VALUES ARE IN uF
1 PART OF ASSEMBLY NO. 406517

NOTES: UNLESS OTHERWISE SPECIFIED

406049	8134	REF	
406049	8114	REF	
NEXT DWG	USED ON	NEXT DWG	FINAL ASSY
APPLICATION		QTY REQD	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE THICKNESS OF PLATING

TOLERANCES

DECIMALS	ANGLES	HOLE DIAMETERS
X.030	0° 30'	+.004
XX.020	FORMED	-.001
XXX.010	1° 0'	

DIMENSIONS AND TOLERANCES PER USAS Y14.15

MATERIAL / FINISH

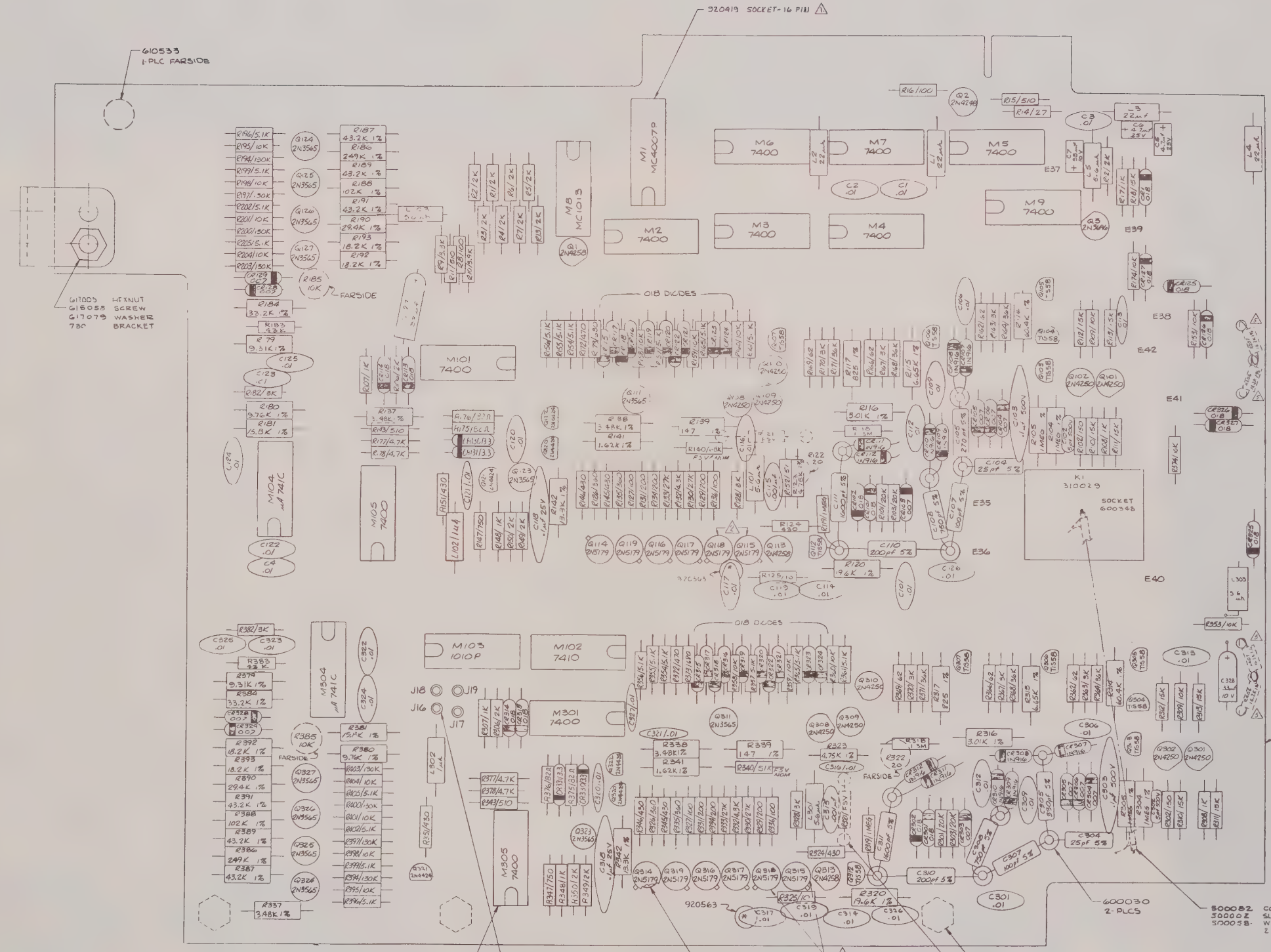
DRAWN	Kuba	1/9/70
CHECK	L. Tingen	6-3-70
DESIGN		
MECH ENGR		
PROJ ENGR	L.R. Mayer	1-13-70
PROD ENGR	B. Sullivan	6-2-70

DANA LABORATORIES INC.
IRVINE, CALIFORNIA

SCHEMATIC PROGRAM SIGNAL CONDITIONER – DUAL

SIZE	CODE IDENT NO	DWG NO.	REV
D	21793	721049	P

SCALE | SHEET 1 OF 3



NOTE:
DO NOT INSTALL
GLASS BEADS
ON DISC CAPACITORS

NOTE:
1. ALL ICS HAVE SOCKETS. ICS TO HAVE SAME ORIENTATION AS SOCKETS
2. Q115 & Q118, Q315 & Q318 ARE MATCHED PAIR PER DANA P/N 200186 TRANS.
3. SCHEMATIC REF. 721049
4. R184, 384, 186, 386, 187, 189, 191, 387, 389, 391, 188, 388, 190, 390, 192, 193, 392, 393 ARE RN55C
5. R204, R207, R406 & R407 TO BE INSTALLED AT NEXT ASSY ON FAR SIDE OF PCB

DANA LABORATORIES INC
IRVINE CALIFORNIA

ASSY - P.C.B.
PROGRAM SIGNAL COND.
DUAL

SIZE	CODE IDENT NO	DWG NO.	REV
	21793	406049	W

SCALE 4:1 SHEET 1 OF 6

REVISIONS				
LTR	DESCRIPTION	DR	CHK	APPD
C	RELEASED PER DRN-, REV. "C"	D		1-13-70

SEE SHEET 1

ATTEN INPUT B
+18V
-18V
AC/DC
Y
X
RMT
$\overline{RMT}$
TRIGGER B
MARKER INPUT B
ANALOG INPUT
+/- SLOPE
PRESET
S4 AC / DC
S5 +/- SLOPE
S7A
S7B
S7C
BEAD
FSV 51K NOMINAL
R321 SELECT (KIT)

NOTES: UNLESS OTHERWISE SPECIFIED

406049	8134	REF	
406049	8114	REF	
NEXT DWG	USED ON	NEXT DWG	FINAL ASSY
APPLICATION		QTY REQD	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE THICKNESS OF PLATING

TOLERANCES

DECIMALS	ANGLES	HOLE DIAMETERS
X.030	0° 30'	+.004
XX.020	FORMED	-.001
XXX.010	1° @	

DIMENSIONS AND TOLERANCES PER USAS Y14.15

MATERIAL / FINISH

DRAWN	Duke	1/2/70
CHECK		
DESIGN		
MECH ENGR		
PROJ ENGR	WR Mayer	1-13-70
PROD ENGR	Rdelmo	6-2-70

DANA DANA LABORATORIES INC. IRVINE, CALIFORNIA

SCHEMATIC — CHAN. B PROGRAM SIGNAL CONDITIONER - DUAL

SIZE	CODE IDENT NO.	DWG NO.	REV
D	21793	721049	P

SCALE — SHEET 3 OF 3

REVISIONS				
LTR	DESCRIPTION	DR	CHK	APPD
	RELEASED PER ~~DWN~~ REV "C"	11-21-70 D		D.R. 1-13-71

SEE SHEET 1

ATTEN INPUT A
+18V
-18V

R102 150
C102 5 pf 500V
C104 25 pf 5%
C107 100 pf 5%
C110 200 pf 5%
R103 20K
R104 1M 1%
R105 1M 1%
C105 27CpF 5%
C108 750 pf 5%
C111 1600 pf 5%
CR103 007
CR104 007
CR105 007
CR106 007
CR107 1N916
CR108 1N916
CR109 1N916
CR110 1N916
CR111 1N916
CR112 1N916
C101 .01
C103 1 500V
C106 .01
C109 .01
C112 .01
R101 20K
CR101 018
CR102
R116 3.01K 1%
R114 60.4K 1%
R115 6.65K 1%
R117 825 1%
R118 1.3 M
Q104 TIS58 200173
Q105 TIS58 200173
Q106 TIS58 200173
Q107 TIS58 200173
Q103 TIS58 200173
C116 .01
R119 1M
R121 SELECT (KIT)
R122 20
R123 4.75K 1%
CW
L101 5.6 uh
R125 10
C126 .01
R120 19.6K 1%
C114 .01
Q112 TIS58 200173
Q113 2N4258
Q114 2N5179
Q115 2N5179
R124 430
R152 51
C115 .001
R126 360
R127 100
R128 3K
R129 200
R130 27K
R133 27K
R134 200
Q119 2N5179
C119 .01
+18V
+5V
R147 750
R149 2K
R131 200
R135 360
R140 FSV 68K NOMINAL
R141 1.62K 1%
R142 13.3K 1%
R144 25K CW
R206 16.2K 1%
R205 16.2K 1%
Q116 2N5179
Q117 2N5179
R136 100
BEAD
Q118 2N5179
Q121 2N4424
C117 .01
C121 .01
R132 4.3K
R138 3.48K 1%
R139 147 1%
R137 3.45K 1%
R145 430
R146 430
R148 1K
R150 2K
R151 430
Q123 2N3565
L102 1uh
M103 1010P
M103 1010P
J17
J16 TRIGGER A
MARKER INPUT A
E19 ANALOG INPUT
C118 25V
Q122 2N4424
Q121 2N4424
+5V PRESET
S6B
R143 510
-18V
R179 9.31K 1%
R180 9.76K 1%
R181 15.8 K 1%
C124 .01
R183 43K
C125 .01
R185 10K
R184 33.2K 1%
CR128 007
R186 249K 1%
R187 43.2K 1%
Q124 2N3565
R188 102K 1%
R189 43.2K 1%
Q125 2N3565
R190 29.4K 1%
R191 43.2K 1%
Q126 2N3565
R192 18.2K 1%
R193 18.2K 1%
Q127 2N3565
CR129 007
+18V
R194 130K
R195 10K
R196 5.1K
R197 130K
R198 10K
R199 5.1K
R200 130K
R201 10K
R202 5.1K
R203 130K
R204 10K
R205 5.1K
E10 P
E9 N
E11 M
E12 L
C122 .01 +18V
M104 741C
C123 .01
R182 3K
-18V
R108 1K
R109 10K
Q102 2N4250
R110 15K
R111 15K
Q101 2N4250
R112 15K
R113 15K
R107 1K
R106 2K
C113 .01
-18V
+5V
Q108 2N4250
Q111 2N3565
R172 470
R173 680
R162 62
R163 3K
R164 36K
Q109 2N4250
R165 5.1K
R166 62
R167 3K
R168 36K
Q110 2N4250
R169 62
R170 3K
R171 36K
R157 5.1K
R158 10K
R159 10K
R160 10K
R161 5.1K
CR113 018
CR114 018
CR115 018
CR116 018
CR117 018
CR118 018
CR119 018
CR120 108
CR121 018
CR122 018
CR123 018
CR124 018
R155 5.1K
R154 5.1K
R156 5.1K
+5V
PRESET 0.1 1 10 100
S6A
AC/DC E20
DC AC
S1 AC/DC
E38
E37
R153 10K
+5V
-18V
Y E25
X E7
RMT
$\overline{RMT}$
M101 7400
M101 7400
M101 7400
M102 7410
M107 7410
CR125 018
CR126 018
CR127 018
R174 10K
M105 7400
M105 7400
M105 7400
M105 7400
S6C PRESET
S2 +/- SLOPE
E39
+5V
R175 82Ω
R176 82Ω
CR130 3.3V
CR131 3.3V
C121 .01
R177 4.7K
R178 4.7K
-18V
E26 +/- SLOPE

NOTES: UNLESS OTHERWISE SPECIFIED

406049	8134	REF	
406049	8114	REF	
NEXT DWG	USED ON	NEXT DWG	FINAL ASSY
APPLICATION		QTY REQD	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE THICKNESS OF PLATING

TOLERANCES

DECIMALS	ANGLES	HOLE DIAMETERS
X.030	0° 30'	+.004
XX.020	FORMED	-.001
XXX.010	1° 0'	

DIMENSIONS AND TOLERANCES PER USAS Y14.15

MATERIAL / FINISH

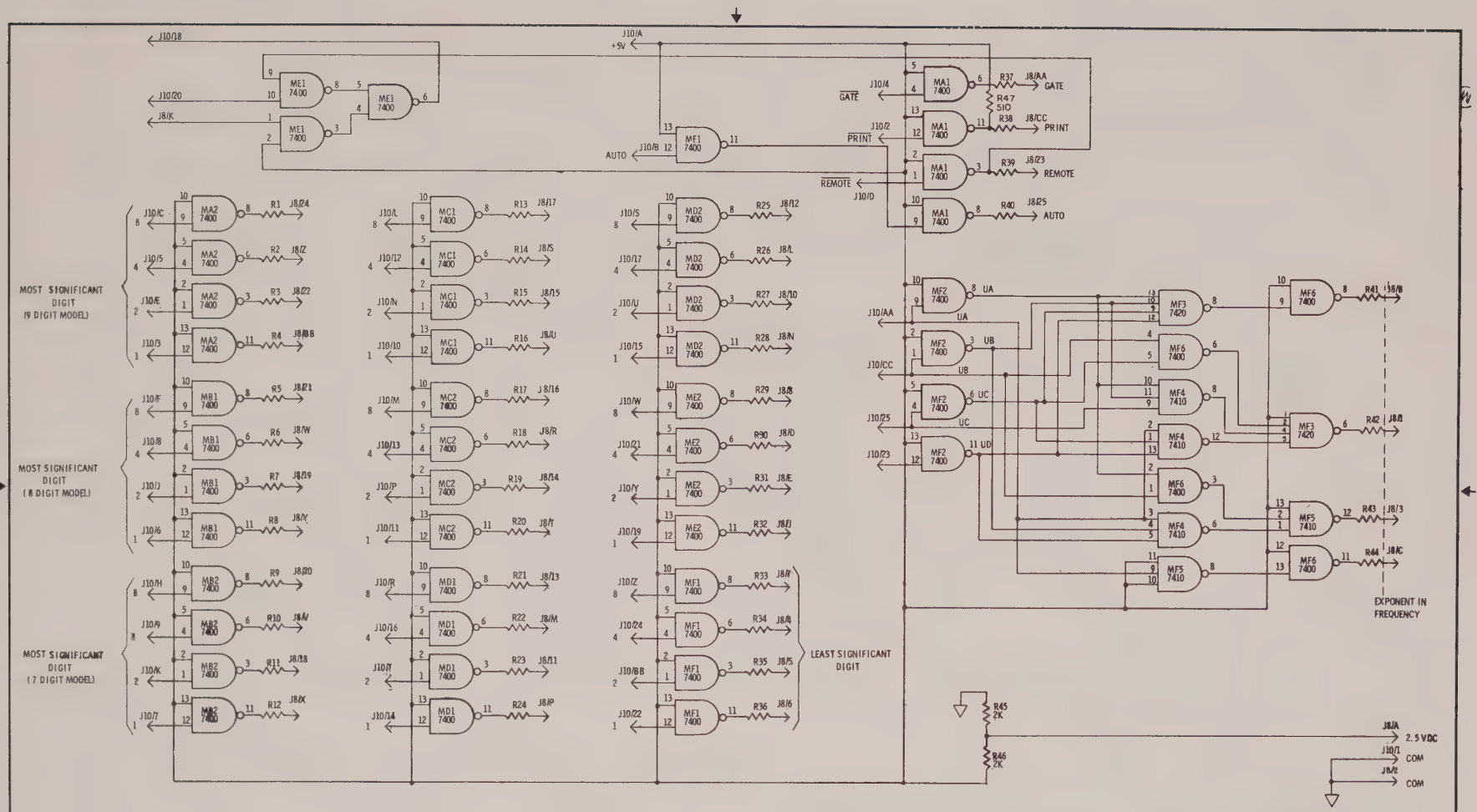
DRAWN	Duke	1/16/70
CHECK		
DESIGN		
MECH ENGR		
PROJ ENGR	W.R. Mayer	1-13-71
PROD ENGR	B. Solano	6-2-70

DANA LABORATORIES INC.
IRVINE, CALIFORNIA

SCHEMATIC —— CHAN. A
PROGRAM SIGNAL
CONDITIONER – DUAL

SIZE	CODE IDENT NO.	DWG NO.	REV
D	21793	721049	P

SCALE | SHEET 2 OF 3



3. PIN 7 ALL I.C.'S TO COMMON GROUND
2. Vcc = +5VDC. TO PINS 14 ALL I C S
1. ALL RESISTORS ARE 39 OHM, 1/4 W, 5%

NOTES: UNLESS OTHERWISE SPECIFIED

406050	OPTION 500	EXP	REF
NEXT DWG	USED ON	NEXT DWG	FINAL ASSY
APPLICATION		QTY REQD	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE THICKNESS OF PLATING

TOLERANCES

DECIMALS	ANGLES	HOLE DIAMETERS
X.030	0° 30'	- .004
XX.020	FORMED	- .001
XXX.010	1° 0'	

DIMENSIONS AND TOLERANCES PER USAS Y14.15

MATERIAL | FINISH

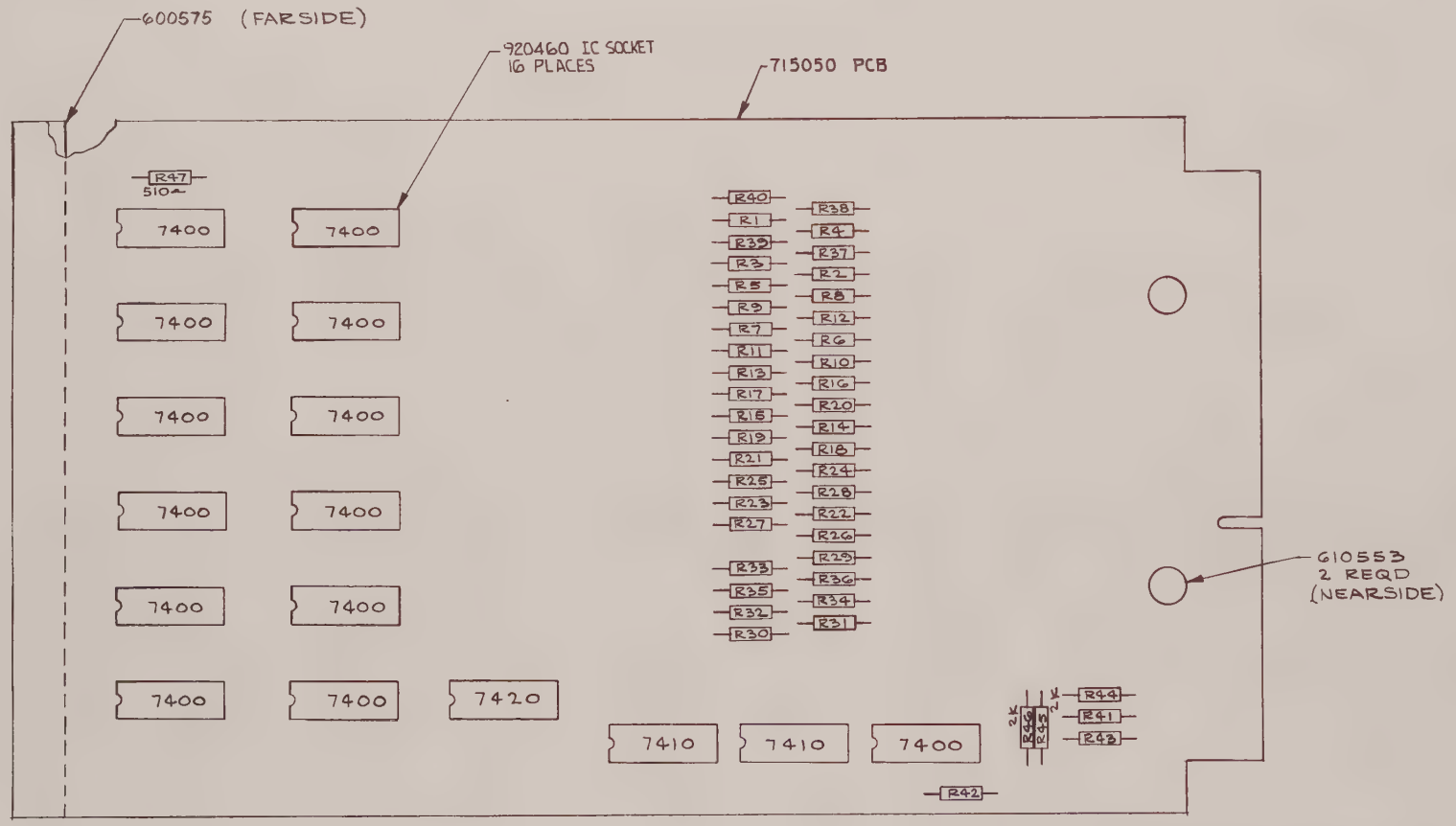
DRAWN	C. WARNER	19 NOV 1969
CHECK	W R Morgan	20 NOV 69
DESIGN		
MECH ENGR		
PROJ ENGR	W Morgan	6-2-70
PROD ENGR	P Salerno	6-3-70

DANA LABORATORIES INC.
IRVINE, CALIFORNIA

SCHEMATIC - ELECTRICAL OUTPUT

SIZE	CODE IDENT NO.	DWG NO.	REV
D	21793	721050	C

SCALE —— SHEET 1 OF 1



2. ALL I.C. HAVE SOCKETS

1. ALL RESISTORS ARE 1/4W
± 39 OHMS ± 5 %

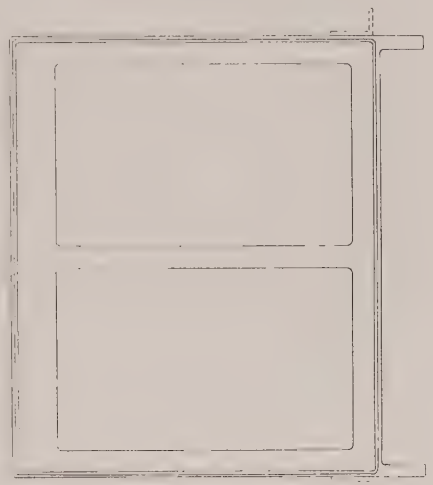
NOTES: UNLESS OTHERWISE SPECIFIED

DANA LABORATORIES INC.
IRVINE, CALIFORNIA

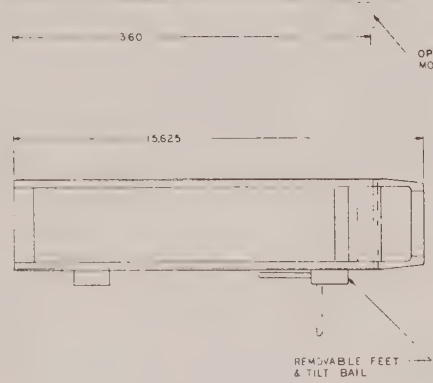
ASSY P.C. BOARD-ELECTRICAL OUTPUT

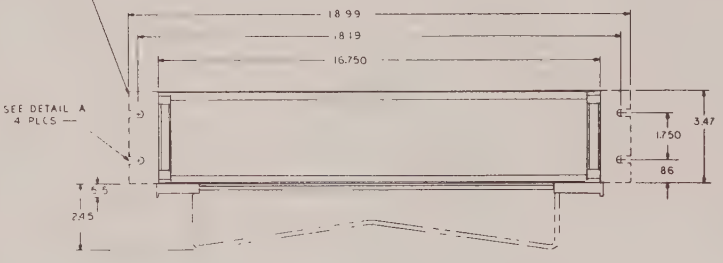
SIZE	CODE IDENT NO.	DWG NO.	REV
C	21793	406050	L

SCALE 2/1 SHEET 1 OF 2



DETAIL A
SCALE: 2/1





NOTES UNLESS OTHERWISE SPECIFIED

406377	8159	REF	REF
406376	8129		
406375	8119		
406374	8109		
406370	8130		
406371	8120		
406372	8110		
406373	8100	REF	REF
NEXT DWG	USED ON	NEXT DWG	FINAL ASSY
APPLICATION		QTY REQD	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE THICKNESS OF PLATING

TOLERANCES

DECIMALS	ANGLES	HOLE DIAMETERS
.X ±.030	0° 30'	+.004
.XX ±.020	FORMED	-.001
.XXX ±.010	± 1°	

DIMENSIONS AND TOLERANCES PER USAS Y14.5

MATERIAL | FINISH

DRAWN	Aday	1-19-70
CHECK	K. Scott	1-20-70
DESIGN	K. Scott	1-20-70
MECH ENGR		
PROJ ENGR		
PROD ENGR	Ed Salazar	6-2-70

DANA DANA LABORATORIES INC.
IRVINE, CALIFORNIA

DIMENSIONAL OUTLINE - SERIES 8100 COUNTER

SIZE	CODE IDENT NO	DWG NO.	REV
D	21793	730350	A

SCALE 1/2 SHEET 1 OF 1

SECTION 9 PARTS LIST

9.1 This section contains lists of replaceable parts arranged in the order of the following sub-assemblies:

	Page
Power Supply	9-3
Units Display	9-4
Readout 8 Digit	9-5
Readout 9 Digit	9-10
High Speed Switching	9-11
50 MHz Preamp Single	9-15
50 MHz Preamp Dual	9-17
500 MHz Prescaler	9-22
Program Signal Conditioner – Single	9-29
Program Signal Conditioner – Dual	9-35
Electrical Output	9-46

9.2 Manufacturers are identified by FSC numbers listed in table 9.2, "List of Suppliers". The code numbers are from the Federal Supply Code for Manufacturers Cataloging Handbooks H4-1, H4-2, and their supplements.

9.3 Certain parts having 21793 (Dana) listed in the "FSC" column are specially-selected semiconductors. For some of these, standard commercial parts will serve as satisfactory replacements. These Dana parts are identified in table 9.1 along with the commercial equivalent.

Table 9.1

Semiconductor Type:		Equivalent:
007	Diode	Fairchild FD300
018	Diode	Texas Instruments 1N4448
021	Transistor	MPS A92

Table 9.2 - List of Suppliers

FSC	NAME
01295	TEXAS INSTRUMENTS, INC. (Components Group) DALLAS, TEXAS
04713	MOTOROLA, INC. (Semiconductor Products Division) PHOENIX, ARIZONA
05397	UNION CARBIDE CORP. (Materials Systems Division) CLEVELAND, OHIO
07263	FAIRCHILD SEMICONDUCTOR (Division of Fairchild Camera & Instrument Corp.) MOUNTAIN VIEW, CALIFORNIA
07716	TRW ELECTRONIC COMPONENTS (IRC) BURLINGTON, IOWA
09023	CORNELL-DUBILEAR ELECTRONICS (Division Federal Pacific Electric Co.) SANFORD, NORTH CAROLINA
20754	KMC SEMICONDUCTOR CORP. LONG VALLEY, NEW JERSEY
21793	DANA LABORATORIES, INC. IRVINE, CALIFORNIA
26806	AMERICAN ZETTLER, INC. COSTA MESA, CALIFORNIA
27556	IMB ELECTRONIC PRODUCTS, INC. SANTA FE SPRINGS, CALIFORNIA
50434	HEWLETT-PACKARD CO. (HP Associates) PALO ALTO, CALIFORNIA
56289	SPRAGUE ELECTRIC CO. (Pacific Division) LOS ANGELES, CALIFORNIA
71471	AEROVOX CORP. (Cinema Plant) MONCKS CORNER, SOUTH CAROLINA
71590	CENTRALAB ELECTRONICS (Division of Globe-Union, Inc.) MILWAUKEE, WISCONSIN
72136	ELECTRO MOTIVE MFG. CO., INC. WILLIMANTIC, CONNECTICUT
72982	ERIE TECHNOLOGICAL PRODUCTS, INC. ERIE, PENNSYLVANIA
73138	BECKMAN INSTRUMENTS, INC. (Helipot Division) FULLERTON, CALIFORNIA
73445	AMPEREX ELECTRONIC CORP. HICKSVILLE, LONG ISLAND, NEW YORK
76493	J.W. MILLER CO. COMPTON, CALIFORNIA
80131	ELECTRONICS INDUSTRIES ASSOC. WASHINGTON, D.C.
81349	MILITARY SPECIFICATION
83125	NYTRONICS, INC. (Capacitor Division) DARLINGTON, SOUTH CAROLINA
98291	SEALECTRO CORP. MAMARONECK, NEW YORK
99800	AMERICAN PRECISION INDUSTRIES, INC. (Delevan Division) EAST AURORA, NEW YORK

406043 – Assy., PCB, POWER SUPPLY

REF DES	DANA P/N	DESCRIPTION					FSC	MANU P/N
C1	110133	CAP	ELECT	1100 MFD	50 V		56289	39D118G050HP4
C2	110062	CAP	ELECT	500 MFD	50 V		56289	39D507G050GL4
C3	110131	CAP	ELECT	20 MFD	450 V		56289	39D206F450GL4
C4	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C5	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C6	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C7	110001	CAP	TANTA	6.8 MFD	35 V	10%	05397	T310B685K035AS
C8	110001	CAP	TANTA	6.8 MFD	35 V	10%	05397	T310B685K035AS
C9	110001	CAP	TANTA	6.8 MFD	35 V	10%	05397	T310B685K035AS
C10	110001	CAP	TANTA	6.8 MFD	35 V	10%	05397	T310B685K035AS
C14	100057	CAP	CERAM	.1 MFD	500 V	20%	56289	5GA-P10
CR1	210004	DIODE	SILICO		1N4004		81349	1N4004
CR2	210004	DIODE	SILICO		1N4004		81349	1N4004
CR3	210004	DIODE	SILICO		1N4004		81349	1N4004
CR4	210004	DIODE	SILICO		1N4004		81349	1N4004
CR5	210004	DIODE	SILICO		1N4004		81349	1N4004
CR6	210004	DIODE	SILICO		1N4004		81349	1N4004
CR7	210004	DIODE	SILICO		1N4004		81349	1N4004
CR8	210004	DIODE	SILICO		1N4004		81349	1N4004
M1	230082	INTEGRATED CIRCUIT			MC1461R		04713	MC1461R
M2	230082	INTEGRATED CIRCUIT			MC1461R		04713	MC1461R
M3	230082	INTEGRATED CIRCUIT			MC1461R		04713	MC1461R
R1	000474	RES	CARBON	470 K		5% 1/4W	81349	RC07GF474J
R2	010523	RES	METAL	13 K		1% 1/4W	81349	RN60D1302F
R3	010590	RES	METAL	18.2 K		1% 1/4W	81349	RN60D
R4	010589	RES	METAL	2.55 K		1% 1/4W	81349	RN60D2551F
R5	040049	POT	CERMET	2 K	89WV2K		73138	89WV2K
R6	010214	RES	METAL	5.11 K	T-0	1%	81349	RN60D5111F
R7	010590	RES	METAL	18.2 K		1% 1/4W	81349	RN60D
R8	010523	RES	METAL	13 K		1% 1/4W	81349	RN60D1302F
R9	001768	RES	CARBON	3.3 OHM		5% 1/4W		
R10	000331	RES	CARBON	330 OHM		5% 1/4W	81349	RC07GF331J
R11	001771	RES	CARBON	1.8 OHM		5% 1/2W		
R12	001724	RES	CARBON	1.0 OHM		5% 1/2W		
R13	000471	RES	CARBON	470 OHM		5% 1/4W	81349	RC07GF471J
R14	001695	RES	CARBON	200 OHM		5% 1/2W	81349	RC20GF201J
R15	000220	RES	CARBON	22 OHM		5% 1/4W	81349	RC07GF220J

406055 – Assy., PCB, UNITS DISPLAY

REF DES	DANA P/N	DESCRIPTION					FSC	MANU P/N
CR16	220056	DIODE	ZENER		75 V	5%	81349	1N982B
DS1	920116	LAMP	NEON		NE-2H			MPG250-3
DS2	920116	LAMP	NEON		NE-2H			MPG250-3
DS3	920116	LAMP	NEON		NE-2H			MPG250-3
DS4	920116	LAMP	NEON		NE-2H			MPG250-3
DS5	920116	LAMP	NEON		NE-2H			MPG250-3
DS6	920116	LAMP	NEON		NE-2H			MPG250-3
DS7	920116	LAMP	NEON		NE-2H			MPG250-3
R69	000104	RES	CARBON	100 K		5% 1/4W	81349	RC07GF104J
R70	000104	RES	CARBON	100 K		5% 1/4W	81349	RC07GF104J
R73	000393	RES	CARBON	39 K		5% 1/4W	81349	RC07GF393J
R74	000393	RES	CARBON	39 K		5% 1/4W	81349	RC07GF393J
R77	000100	RES	CARBON	10 OHM		5% 1/4W	81349	RC07GF100J
R80	000100	RES	CARBON	10 OHM		5% 1/4W	81349	RC07GF100J
R83	000100	RES	CARBON	10 OHM		5% 1/4W	81349	RC07GF100J
R86	000105	RES	CARBON	1 M		5% 1/4W	81349	RC07GF105J
R87	000105	RES	CARBON	1 M		5% 1/4W	81349	RC07GF105J

406046 – Assy., PCB, READOUT 8 DIGIT

REF DES	DANA P/N	DESCRIPTION					FSC	MANU P/N
C1	100063	CAP	CERAM	.01 MFD	500 V	20%	56289	5GAS-S10
C2	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C3	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C4	100009	CAP	CERAM	5 PFD		10%	71471	TCDI-1 (N750)
C5	100053	CAP	CERAM	56 PFD	1000 V	5%	56289	10TCCQ56
C6	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C7	100050	CAP	CERAM	2.2 PFD	1000 V	5%	56289	10TCCV22
C8	100051	CAP	CERAM	3 PFD	500 V		71471	TCD-B1-0
C9	100060	CAP	CERAM	15 PFD	1000 V	5%	56289	10TCCQ15
C10	100049	CAP	CERAM	100 PFD	1000 V	5%	56289	10TCCT10
C11	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C12	101174	CAP	CERAM	.001 MFD	500 V	10%	71471	SCD3X5F
C13	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C14	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C15	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C16	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C17	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C18	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C19	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C20	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C21	100063	CAP	CERAM	.01 MFD	500 V	20%	56289	5GAS-S10
C22	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C23	120048	CAP	MYLAR	.068 MFD	200 V	10%	27556	ZA2C683K
C24	110126	CAP	TANTA	6.8 MFD	35 V		05397	T368B685M035AS
CR1	211083	DIODE	SILICO		018		21793	211083
CR2	211083	DIODE	SILICO		018		21793	211083
CR3	211083	DIODE	SILICO		018		21793	211083
CR4	211083	DIODE	SILICO		018		21793	211083
CR5	211083	DIODE	SILICO		018		21793	211083
CR6	211083	DIODE	SILICO		018		21793	211083
CR8	211083	DIODE	SILICO		018		21793	211083
CR9	211083	DIODE	SILICO		018		21793	211083
CR10	211083	DIODE	SILICO		018		21793	211083
CR12	211083	DIODE	SILICO		018		21793	211083
CR13	211083	DIODE	SILICO		018		21793	211083
CR15	211083	DIODE	SILICO		018		21793	211083
CR16	211083	DIODE	SILICO		018		21793	211083
L1	310072	CHOKE	RF	2.2 μH		10%	99800	1537-20

406046 – Assy., PCB, READOUT 8 DIGIT *continued*

REF DES	DANA P/N	DESCRIPTION		FSC	MANU P/N
A5	230028	INTEGRATED CIRCUIT	SN7400N	01295	SN7400N
A6	230072	INTEGRATED CIRCUIT	SN7474N	01295	SN7474N
A7	230032	INTEGRATED CIRCUIT	SN7420N	01295	SN7420N
A8	230030	INTEGRATED CIRCUIT	SN7402N	01295	SN7402N
A9	230030	INTEGRATED CIRCUIT	SN7402N	01295	SN7402N
A10	230028	INTEGRATED CIRCUIT	SN7400N	01295	SN7400N
B1	230028	INTEGRATED CIRCUIT	SN7400N	01295	SN7400N
B2	230028	INTEGRATED CIRCUIT	SN7400N	01295	SN7400N
B3	230037	INTEGRATED CIRCUIT	SN7490N	01295	SN7490N
B4	230028	INTEGRATED CIRCUIT	SN7400N	01295	SN7400N
B5	230028	INTEGRATED CIRCUIT	SN7400N	01295	SN7400N
B6	230028	INTEGRATED CIRCUIT	SN7400N	01295	SN7400N
B7	230080	INTEGRATED CIRCUIT	SN7496N	01295	SN7496N
B8	230080	INTEGRATED CIRCUIT	SN7496N	01295	SN7496N
B9	230080	INTEGRATED CIRCUIT	SN7496N	01295	SN7496N
B10	230080	INTEGRATED CIRCUIT	SN7496N	01295	SN7496N
C1	230028	INTEGRATED CIRCUIT	SN7400N	01295	SN7400N
C2	230031	INTEGRATED CIRCUIT	SN7410N	01295	SN7410N
C3	230031	INTEGRATED CIRCUIT	SN7410N	01295	SN7410N
C4	230074	INTEGRATED CIRCUIT	SN7442N	07716	SN7442N
C5	230037	INTEGRATED CIRCUIT	SN7490N	01295	SN7490N
C6	230030	INTEGRATED CIRCUIT	SN7402N	01295	SN7402N
C7	230028	INTEGRATED CIRCUIT	SN7400N	01295	SN7400N
C8	230028	INTEGRATED CIRCUIT	SN7400N	01295	SN7400N
C9	230028	INTEGRATED CIRCUIT	SN7400N	01295	SN7400N
C10	230028	INTEGRATED CIRCUIT	SN7400N	01295	SN7400N
D6	230030	INTEGRATED CIRCUIT	SN7402N	01295	SN7402N
D7	230031	INTEGRATED CIRCUIT	SN7410N	01295	SN7410N
D8	230031	INTEGRATED CIRCUIT	SN7410N	01295	SN7410N
D9	230031	INTEGRATED CIRCUIT	SN7410N	01295	SN7410N
D10	230028	INTEGRATED CIRCUIT	SN7400N	01295	SN7400N
E12	230065	INTEGRATED CIRCUIT	SN7475N	01295	SN7475N
E13	230065	INTEGRATED CIRCUIT	SN7475N	01295	SN7475N
E14	230065	INTEGRATED CIRCUIT	SN7475N	01295	SN7475N
E15	230065	INTEGRATED CIRCUIT	SN7475N	01295	SN7475N
E16	230065	INTEGRATED CIRCUIT	SN7475N	01295	SN7475N
E17	230065	INTEGRATED CIRCUIT	SN7475N	01295	SN7475N
E18	230065	INTEGRATED CIRCUIT	SN7475N	01295	SN7475N
E19	230065	INTEGRATED CIRCUIT	SN7475N	01295	SN7475N
F12	230034	INTEGRATED CIRCUIT	SN74141N	01295	SN74141N
F13	230034	INTEGRATED CIRCUIT	SN74141N	01295	SN74141N
F14	230034	INTEGRATED CIRCUIT	SN74141N	01295	SN74141N

406046 – Assy., PCB, READOUT 8 DIGIT *continued*

REF DES	DANA P/N	DESCRIPTION	FSC	MANU P/N
F15	230034	INTEGRATED CIRCUIT SN74141N	01295	SN74141N
F16	230034	INTEGRATED CIRCUIT SN74141N	01295	SN74141N
F17	230034	INTEGRATED CIRCUIT SN74141N	01295	SN74141N
F18	230034	INTEGRATED CIRCUIT SN74141N	01295	SN74141N
F19	230034	INTEGRATED CIRCUIT SN74141N	01295	SN74141N
Q1	200037	TRANS SILICO NPN 2N3646	80131	2N3646
Q2	200037	TRANS SILICO NPN 2N3646	80131	2N3646
Q3	200037	TRANS SILICO NPN 2N3646	80131	2N3646
Q4	200037	TRANS SILICO NPN 2N3646	80131	2N3646
Q5	200037	TRANS SILICO NPN 2N3646	80131	2N3646
Q6	200037	TRANS SILICO NPN 2N3646	80131	2N3646
Q7	200037	TRANS SILICO NPN 2N3646	80131	2N3646
Q8	200037	TRANS SILICO NPN 2N3646	80131	2N3646
Q9	200043	TRANS 200043	21793	200043
Q10	200043	TRANS 200043	21793	200043
Q11	200087	TRANS SILICO 021	21793	200087
Q12	200087	TRANS SILICO 021	21793	200087
Q13	200087	TRANS SILICO 021	21793	200087
Q15	200087	TRANS SILICO 021	21793	200087
Q16	200087	TRANS SILICO 021	21793	200087
Q17	200087	TRANS SILICO 021	21793	200087
Q18	200087	TRANS SILICO 021	21793	200087
Q19	200087	TRANS SILICO 021	21793	200087
Q20	200087	TRANS SILICO 021	21793	200087
Q21	200087	TRANS SILICO 021	21793	200087
Q22	200087	TRANS SILICO 021	21793	200087
R1	000510	RES CARBON 51 OHM 5% 1/4W	81349	RC07GF510J
R2	000122	RES CARBON 1.2 K 5% 1/4W	81349	RC07GF122J
R3	000472	RES CARBON 4.7 K 5% 1/4W	81349	RC07GF472J
R4	000752	RES CARBON 7.5 K 5% 1/4W	81349	RC07GF752J
R5	000751	RES CARBON 750 OHM 5% 1/4W	81349	RC07GF751J
R6	000102	RES CARBON 1 K 5% 1/4W	81349	RC07GF102J
R7	000221	RES CARBON 220 OHM 5% 1/4W	81349	RC07GF221J
R8	000562	RES CARBON 5.6 K 5% 1/4W	81349	RC07GF562J
R9	000102	RES CARBON 1 K 5% 1/4W	81349	RC07GF102J
R10	000102	RES CARBON 1 K 5% 1/4W	81349	RC07GF102J
R11	000101	RES CARBON 100 OHM 5% 1/4W	81349	RC07GF101J
R12	000332	RES CARBON 3.3 K 5% 1/4W	81349	RC07GF332J
R13	000153	RES CARBON 15 K 5% 1/4W	81349	RC07GF153J
R14	000302	RES CARBON 3 K 5% 1/4W	81349	RC07GF302J

406046 – Assy., PCB, READOUT 8 DIGIT *continued*

REF DES	DANA P/N	DESCRIPTION				FSC	MANU P/N
R15	000102	RES	CARBON	1 K	5% 1/4W	81349	RC07GF102J
R16	000302	RES	CARBON	3 K	5% 1/4W	81349	RC07GF302J
R17	000152	RES	CARBON	1.5 K	5% 1/4W	81349	RC07GF152J
R18	000100	RES	CARBON	10 OHM	5% 1/4W	81349	RC07GF100J
R19	000303	RES	CARBON	30 K	5% 1/4W	81349	RC07GF303J
R20	000202	RES	CARBON	2 K	5% 1/4W	81349	RC07GF202J
R21	000202	RES	CARBON	2 K	5% 1/4W	81349	RC07GF202J
R22	000101	RES	CARBON	100 OHM	5% 1/4W	81349	RC07GF101J
R23	000183	RES	CARBON	18 K	5% 1/4W	81349	RC07GF183J
R24	000202	RES	CARBON	2 K	5% 1/4W	81349	RC07GF202J
R25	000202	RES	CARBON	2 K	5% 1/4W	81349	RC07GF202J
R26	000201	RES	CARBON	200 OHM	5% 1/4W	81349	RC07GF201J
R27	000203	RES	CARBON	20 K	5% 1/4W	81349	RC07GF203J
R28	000302	RES	CARBON	3 K	5% 1/4W	81349	RC07GF302J
R29	000512	RES	CARBON	5.1 K	5% 1/4W	81349	RC07GF512J
R30	000561	RES	CARBON	560 OHM	5% 1/4W	81349	RC07GF561J
R31	000163	RES	CARBON	16 K	5% 1/4W	81349	RC07GF163J
R32	000202	RES	CARBON	2 K	5% 1/4W	81349	RC07GF202J
R33	000302	RES	CARBON	3 K	5% 1/4W	81349	RC07GF302J
R34	000301	RES	CARBON	300 OHM	5% 1/4W	81349	RC07GF301J
R35	000222	RES	CARBON	2.2 K	5% 1/4W	81349	RC07GF222J
R36	000103	RES	CARBON	10 K	5% 1/4W	81349	RC07GF103J
R37	000512	RES	CARBON	5.1 K	5% 1/4W	81349	RC07GF512J
R38	000821	RES	CARBON	820 OHM	5% 1/4W	81349	RC07GF821J
R39	000432	RES	CARBON	4.3 K	5% 1/4W	81349	RC07GF432J
R40	000562	RES	CARBON	5.6 K	5% 1/4W	81349	RC07GF562J
R41	000511	RES	CARBON	510 OHM	5% 1/4W	81349	RC07GF511J
R42	000332	RES	CARBON	3.3 K	5% 1/4W	81349	RC07GF332J
R43	000152	RES	CARBON	1.5 K	5% 1/4W	81349	RC07GF152J
R44	000752	RES	CARBON	7.5 K	5% 1/4W	81349	RC07GF752J
R45	000200	RES	CARBON	20 OHM	5% 1/4W	81349	RC07GF200J
R47	020587	RES	WW	39 K	5% 1/2W	21793	020587
R48	020587	RES	WW	39 K	5% 1/2W	21793	020587
R49	020587	RES	WW	39 K	5% 1/2W	21793	020587
R50	020587	RES	WW	39 K	5% 1/2W	21793	020587
R51	020587	RES	WW	39 K	5% 1/2W	21793	020587
R52	020587	RES	WW	39 K	5% 1/2W	21793	020587
R53	020587	RES	WW	39 K	5% 1/2W	21793	020587
R54	020587	RES	WW	39 K	5% 1/2W	21793	020587
R55	000561	RES	CARBON	560 OHM	5% 1/4W	81349	RC07GF561J
R56	000822	RES	CARBON	8.2 K	5% 1/4W	81349	RC07GF822J
R57	000561	RES	CARBON	560 OHM	5% 1/4W	81349	RC07GF561J

406046 -- Assy., PCB, READOUT 8 DIGIT *continued*

REF DES	DANA P/N	DESCRIPTION				FSC	MANU P/N
R58	000822	RES	CARBON	8.2 K	5% 1/4W	81349	RC07GF822J
R59	000561	RES	CARBON	560 OHM	5% 1/4W	81349	RC07GF561J
R60	000822	RES	CARBON	8.2 K	5% 1/4W	81349	RC07GF822J
R63	000432	RES	CARBON	4.3 K	5% 1/4W	81349	RC07GF432J
R64	000822	RES	CARBON	8.2 K	5% 1/4W	81349	RC07GF822J
R65	000432	RES	CARBON	4.3 K	5% 1/4W	81349	RC07GF432J
R66	000822	RES	CARBON	8.2 K	5% 1/4W	81349	RC07GF822J
R67	000432	RES	CARBON	4.3 K	5% 1/4W	81349	RC07GF432J
R68	000822	RES	CARBON	8.2 K	5% 1/4W	81349	RC07GF822J
R71	000822	RES	CARBON	8.2 K	5% 1/4W	81349	RC07GF822J
R72	000152	RES	CARBON	1.5 K	5% 1/4W	81349	RC07GF152J
R75	000822	RES	CARBON	8.2 K	5% 1/4W	81349	RC07GF822J
R76	000102	RES	CARBON	1 K	5% 1/4W	81349	RC07GF102J
R78	000822	RES	CARBON	8.2 K	5% 1/4W	81349	RC07GF822J
R79	000202	RES	CARBON	2 K	5% 1/4W	81349	RC07GF202J
R81	000822	RES	CARBON	8.2 K	5% 1/4W	81349	RC07GF822J
R82	000202	RES	CARBON	2 K	5% 1/4W	81349	RC07GF202J
R84	000822	RES	CARBON	8.2 K	5% 1/4W	81349	RC07GF822J
R85	000202	RES	CARBON	2 K	5% 1/4W	81349	RC07GF202J
V1	920506	TUBE	NEON DISPLAY	ZM1000		73445	ZM1000
V2	920506	TUBE	NEON DISPLAY	ZM1000		73445	ZM1000
V3	920506	TUBE	NEON DISPLAY	ZM1000		73445	ZM1000
V4	920506	TUBE	NEON DISPLAY	ZM1000		73445	ZM1000
V5	920506	TUBE	NEON DISPLAY	ZM1000		73445	ZM1000
V6	920506	TUBE	NEON DISPLAY	ZM1000		73445	ZM1000
V7	920506	TUBE	NEON DISPLAY	ZM1000		73445	ZM1000
V8	920506	TUBE	NEON DISPLAY	ZM1000		73445	ZM1000
X1	920468	SOCKET	16 PIN INDICATOR	55702		73445	55702
X2	920468	SOCKET	16 PIN INDICATOR	55702		73445	55702
X3	920468	SOCKET	16 PIN INDICATOR	55702		73445	55702
X4	920468	SOCKET	16 PIN INDICATOR	55702		73445	55702
X5	920468	SOCKET	16 PIN INDICATOR	55702		73445	55702
X6	920468	SOCKET	16 PIN INDICATOR	55702		73445	55702
X7	920468	SOCKET	16 PIN INDICATOR	55702		73445	55702
X8	920468	SOCKET	16 PIN INDICATOR	55702		73445	55702
Y1	730240	CRYSTAL		730240		21793	730240

406378 – Assy., PCB, READOUT 9 DIGIT

REF DES	DANA P/N	DESCRIPTION					FSC	MANU P/N
CR7	211083	DIODE	SILICO		018		21793	211083
CR11	211083	DIODE	SILICO		018		21793	211083
CR14	211083	DIODE	SILICO		018		21793	211083
E11	230065	INTEGRATED CIRCUIT			SN7475N		01295	SN7475N
F11	230034	INTEGRATED CIRCUIT			SN74141N		01295	SN74141N
Q14	200087	TRANS	SILICO		021		21793	200087
R46	020587	RES	WW	39 K		5% 1/2W	21793	020587
R61	000822	RES	CARBON	8.2 K		5% 1/4W	81349	RC07GF822J
R62	000561	RES	CARBON	560 OHM		5% 1/4W	81349	RC07GF561J
V9	920506	TUBE	NEON DISPLAY		ZM1000		73445	ZM1000
X9	920468	SOCKET	16 PIN INDICATOR		55702		73445	55702

406081 – Assy., PCB, HIGH SPEED SWITCHING

REF DES	DANA P/N	DESCRIPTION					FSC	MANU P/N
C1	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C2	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C3	110110	CAP	TANTA	6.8 MFD	20 V	10%	05397	T368B685K020AS
C4	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C5	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C6	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C7	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C8	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C9	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C10	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C11	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
CR1	220019	DIODE	SILICO	ZENER	1N752A		81349	1N752A
L1	310070	CHOKE	RF	5.6 μH		10%	99800	1537 Series
A1	230028	INTEGRATED CIRCUIT			SN7400N		01295	SN7400N
A2	230032	INTEGRATED CIRCUIT			SN7420N		01295	SN7420N
A4	230072	INTEGRATED CIRCUIT			SN7474N		01295	SN7474N
A5	230072	INTEGRATED CIRCUIT			SN7474N		01295	SN7474N
A6	230030	INTEGRATED CIRCUIT			SN7402N		01295	SN7402N
A7	230072	INTEGRATED CIRCUIT			SN7474N		01295	SN7474N
B1	230031	INTEGRATED CIRCUIT			SN7410N		01295	SN7410N
B2	230028	INTEGRATED CIRCUIT			SN7400N		01295	SN7400N
B3	230030	INTEGRATED CIRCUIT			SN7402N		01295	SN7402N
B4	230028	INTEGRATED CIRCUIT			SN7400N		01295	SN7400N
B5	230030	INTEGRATED CIRCUIT			SN7402N		01295	SN7402N
B6	230072	INTEGRATED CIRCUIT			SN7474N		01295	SN7474N
B7	230028	INTEGRATED CIRCUIT			SN7400N		01295	SN7400N
C1	230028	INTEGRATED CIRCUIT			SN7400N		01295	SN7400N
C2	230072	INTEGRATED CIRCUIT			SN7474N		01295	SN7474N
C3	230072	INTEGRATED CIRCUIT			SN7474N		01295	SN7474N
C4	230072	INTEGRATED CIRCUIT			SN7474N		01295	SN7474N
C5	230030	INTEGRATED CIRCUIT			SN7402N		01295	SN7402N
C6	230072	INTEGRATED CIRCUIT			SN7474N		01295	SN7474N
C7	230072	INTEGRATED CIRCUIT			SN7474N		01295	SN7474N
D1	230028	INTEGRATED CIRCUIT			SN7400N		01295	SN7400N
D2	230028	INTEGRATED CIRCUIT			SN7400N		01295	SN7400N
D3	230028	INTEGRATED CIRCUIT			SN7400N		01295	SN7400N
D4	230028	INTEGRATED CIRCUIT			SN7400N		01295	SN7400N
D5	230031	INTEGRATED CIRCUIT			SN7410N		01295	SN7410N
D6	230028	INTEGRATED CIRCUIT			SN7400N		01295	SN7400N
D7	230072	INTEGRATED CIRCUIT			SN7474N		01295	SN7474N

406081 – Assy., PCB, HIGH SPEED SWITCHING *continued*

REF DES	DANA P/N	DESCRIPTION		FSC	MANU P/N
E1	230031	INTEGRATED CIRCUIT	SN7410N	01295	SN7410N
E2	230072	INTEGRATED CIRCUIT	SN7474N	01295	SN7474N
E3	230072	INTEGRATED CIRCUIT	SN7474N	01295	SN7474N
E4	230028	INTEGRATED CIRCUIT	SN7400N	01295	SN7400N
E5	230030	INTEGRATED CIRCUIT	SN7402N	01295	SN7402N
E6	230028	INTEGRATED CIRCUIT	SN7400N	01295	SN7400N
E7	230028	INTEGRATED CIRCUIT	SN7400N	01295	SN7400N
F1	230036	INTEGRATED CIRCUIT	SN7483N	01295	SN7483N
F2	230072	INTEGRATED CIRCUIT	SN7474N	01295	SN7474N
F3	230072	INTEGRATED CIRCUIT	SN7474N	01295	SN7474N
F4	230028	INTEGRATED CIRCUIT	SN7400N	01295	SN7400N
F5	230030	INTEGRATED CIRCUIT	SN7402N	01295	SN7402N
F7	230040	INTEGRATED CIRCUIT	MC1013P	04713	MC1013P
G1	230028	INTEGRATED CIRCUIT	SN7400N	01295	SN7400N
G2	230078	INTEGRATED CIRCUIT	SN7491N	01295	SN7491N
G3	230078	INTEGRATED CIRCUIT	SN7491N	01295	SN7491N
G4	230028	INTEGRATED CIRCUIT	SN7400N	01295	SN7400N
G5	230072	INTEGRATED CIRCUIT	SN7474N	01295	SN7474N
G7	230040	INTEGRATED CIRCUIT	MC1013P	04713	MC1013P
H1	230036	INTEGRATED CIRCUIT	SN7483N	01295	SN7483N
H2	230078	INTEGRATED CIRCUIT	SN7491N	01295	SN7491N
H3	230078	INTEGRATED CIRCUIT	SN7491N	01295	SN7491N
H4	230037	INTEGRATED CIRCUIT	SN7490N	01295	SN7490N
H5	230030	INTEGRATED CIRCUIT	SN7402N	01295	SN7402N
H7	230040	INTEGRATED CIRCUIT	MC1013P	04713	MC1013P
J1	230072	INTEGRATED CIRCUIT	SN7474N	01295	SN7474N
J2	230072	INTEGRATED CIRCUIT	SN7474N	01295	SN7474N
J3	230072	INTEGRATED CIRCUIT	SN7474N	01295	SN7474N
J4	230028	INTEGRATED CIRCUIT	SN7400N	01295	SN7400N
J5	230037	INTEGRATED CIRCUIT	SN7490N	01295	SN7490N
J7	230040	INTEGRATED CIRCUIT	MC1013P	04713	MC1013P
K1	230036	INTEGRATED CIRCUIT	SN7483N	01295	SN7483N
K2	230072	INTEGRATED CIRCUIT	SN7474N	01295	SN7474N
K3	230072	INTEGRATED CIRCUIT	SN7474N	01295	SN7474N
K4	230028	INTEGRATED CIRCUIT	SN7400N	01295	SN7400N
K5	230037	INTEGRATED CIRCUIT	SN7490N	01295	SN7490N
K6	230043	INTEGRATED CIRCUIT	MC1010P	04713	MC1010P
K7	230041	INTEGRATED CIRCUIT	MC1007P	04713	MC1007P
L1	230028	INTEGRATED CIRCUIT	SN7400N	01295	SN7400N
L2	230078	INTEGRATED CIRCUIT	SN7491N	01295	SN7491N
L3	230078	INTEGRATED CIRCUIT	SN7491N	01295	SN7491N
L4	230028	INTEGRATED CIRCUIT	SN7400N	01295	SN7400N

406081 – Assy., PCB, HIGH SPEED SWITCHING *continued*

REF DES	DANA P/N	DESCRIPTION	FSC	MANU P/N
L5	230030	INTEGRATED CIRCUIT SN7402N	01295	SN7402N
L6	230068	INTEGRATED CIRCUIT MC1022P	04713	MC1022P
L7	230030	INTEGRATED CIRCUIT SN7402N	01295	SN7402N
M1	230028	INTEGRATED CIRCUIT SN7400N	01295	SN7400N
M2	230078	INTEGRATED CIRCUIT SN7491N	01295	SN7491N
M3	230078	INTEGRATED CIRCUIT SN7491N	01295	SN7491N
M4	230030	INTEGRATED CIRCUIT SN7402N	01295	SN7402N
M5	230031	INTEGRATED CIRCUIT SN7410N	01295	SN7410N
M6	230033	INTEGRATED CIRCUIT SN7430N	01295	SN7430N
M7	230028	INTEGRATED CIRCUIT SN7400N	01295	SN7400N
Q1	200099	TRANS 2N4258	81349	2N4258
Q2	200099	TRANS 2N4258	81349	2N4258
Q3	200099	TRANS 2N4258	81349	2N4258
Q4	200099	TRANS 2N4258	81349	2N4258
Q5	200099	TRANS 2N4258	81349	2N4258
Q6	200099	TRANS 2N4258	81349	2N4258
Q7	200099	TRANS 2N4258	81349	2N4258
Q8	200099	TRANS 2N4258	81349	2N4258
R1	000151	RES CARBON 150 OHM 5% 1/4W	81349	RC07GF151J
R2	000300	RES CARBON 30 OHM 5% 1/4W	81349	RC07GF300J
R3	000162	RES CARBON 1.6 K 5% 1/4W	81349	RC07GF162J
R4	000102	RES CARBON 1 K 5% 1/4W	81349	RC07GF102J
R5	000821	RES CARBON 820 OHM 5% 1/4W	81349	RC07GF821J
R6	000821	RES CARBON 820 OHM 5% 1/4W	81349	RC07GF821J
R7	000511	RES CARBON 510 OHM 5% 1/4W	81349	RC07GF511J
R8	000511	RES CARBON 510 OHM 5% 1/4W	81349	RC07GF511J
R9	000511	RES CARBON 510 OHM 5% 1/4W	81349	RC07GF511J
R10	000821	RES CARBON 820 OHM 5% 1/4W	81349	RC07GF821J
R11	000151	RES CARBON 150 OHM 5% 1/4W	81349	RC07GF151J
R12	000151	RES CARBON 150 OHM 5% 1/4W	81349	RC07GF151J
R13	000300	RES CARBON 30 OHM 5% 1/4W	81349	RC07GF300J
R14	000300	RES CARBON 30 OHM 5% 1/4W	81349	RC07GF300J
R15	000111	RES CARBON 110 OHM 5% 1/4W	81349	RC07GF111J
R16	000300	RES CARBON 30 OHM 5% 1/4W	81349	RC07GF300J
R17	000111	RES CARBON 110 OHM 5% 1/4W	81349	RC07GF111J
R18	000300	RES CARBON 30 OHM 5% 1/4W	81349	RC07GF300J
R19	000111	RES CARBON 110 OHM 5% 1/4W	81349	RC07GF111J
R20	000300	RES CARBON 30 OHM 5% 1/4W	81349	RC07GF300J
R21	000111	RES CARBON 110 OHM 5% 1/4W	81349	RC07GF111J
R22	000512	RES CARBON 5.1 K 5% 1/4W	81349	RC07GF512J

406081 – Assy., PCB, HIGH SPEED SWITCHING *continued*

REF DES	DANA P/N	DESCRIPTION				FSC	MANU P/N
R23	000821	RES	CARBON	820 OHM	5% 1/4W	81349	RC07GF821J
R24	000511	RES	CARBON	510 OHM	5% 1/4W	81349	RC07GF511J
R25	000511	RES	CARBON	510 OHM	5% 1/4W	81349	RC07GF511J
R26	000821	RES	CARBON	820 OHM	5% 1/4W	81349	RC07GF821J
R27	000821	RES	CARBON	820 OHM	5% 1/4W	81349	RC07GF821J
R28	000511	RES	CARBON	510 OHM	5% 1/4W	81349	RC07GF511J
R29	000821	RES	CARBON	820 OHM	5% 1/4W	81349	RC07GF821J
R30	000511	RES	CARBON	510 OHM	5% 1/4W	81349	RC07GF511J

406057 – Assy., PCB, 50 MHz PREAMP SINGLE

REF DES	DANA P/N	DESCRIPTION					FSC	MANU P/N
C2	100076	CAP	CERAM	20 PFD	1000 V	5%	56289	10TCCQ20
C3	130094	CAP	MICA	220 PFD	500 V	5%	72136	SCDM10-221J
C4	100029	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C5	100006	CAP	CERAM	10 PFD	500 V		71471	TCDI-1 (N750)
C6	100052	CAP	CERAM	22 PFD	1000 V	5%	56289	10TCCQ22
C7	100052	CAP	CERAM	22 PFD	1000 V	5%	56289	10TCCQ22
C8	130093	CAP	MICA	200 PFD	500 V	5%	72136	SCDM10-201J
C9	101641	CAP	CERAM	470 PFD		10%	71471	SCD1X5F
C10	100009	CAP	CERAM	5 PFD		10%	71471	TCDI-1 (N750)
C11	101174	CAP	CERAM	.001 MFD	500 V	10%	71471	SCD3X5F
C12	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C13	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C14	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C15	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C16	110001	CAP	TANTA	6.8 MFD	35 V	10%	05397	T310B685K035AS
C17	110135	CAP	TANTA	33 MFD	10 V	10%	56289	150D336X9010B2
C18	110001	CAP	TANTA	6.8 MFD	35 V	10%	05397	T310B685K035AS
C19	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C20	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
CR1	211236	DIODE	SILICO		007		21793	211236
CR2	211083	DIODE	SILICO		018		21793	211083
CR3	211236	DIODE	SILICO		007		21793	211236
CR4	211083	DIODE	SILICO		018		21793	211083
L1	310071	CHOKE	RF	10 μH		10%	21793	200173
L2	310068	CHOKE	RF	1 μH		10%	99800	1537-12
L3	310062	CHOKE	RF	22 μH		10%	21793	200186
L4	310070	CHOKE	RF	5.6 μH		10%	99800	1537 Series
L5	310062	CHOKE	RF	22 μH		10%	99800	1537-44
M1	230043	INTEGRATED CIRCUIT			MC1010P		04713	MC1010P
Q1	200173	TRANS		MATCHED SET			71785	TIS58
Q2	200099	TRANS			2N4258		81349	2N4258
Q3	200186	TRANS		MATCHED SET WITH Q8			81349	2N5179
Q4	200151	TRANS	SILICO		2N5179		81349	2N5179
Q5	200151	TRANS	SILICO		2N5179		81349	2N5179
Q6	200151	TRANS	SILICO		2N5179		81349	2N5179
Q7	200151	TRANS	SILICO		2N5179		81349	2N5179
Q8	200186	TRANS		MATCHED SET WITH Q3			21793	200186

406057 – Assy., PCB, 50 MHz PREAMP SINGLE *continued*

REF DES	DANA P/N	DESCRIPTION					FSC	MANU P/N
R1	000106	RES	CARBON	10 M		5% 1/4W	81349	RC07GF106J
R2	010091	RES	METAL	11 K	T-0	1%	81349	RN60D1102F
R3	010329	RES	METAL	887 K	T-0	1%	81349	RN60D8873F
R4	010317	RES	METAL	90.9 K		1%	81349	RN60D9092F
R5	010317	RES	METAL	90.9 K		1%	81349	RN60D9092F
R6	010060	RES	METAL	10 K	T-0	1%	81349	RN60D1002F
R7	000203	RES	CARBON	20 K		5% 1/4W	81349	RC07GF203J
R8	000824	RES	CARBON	820 K		5% 1/4W	81349	RC07GF824J
R9	000151	RES	CARBON	150 OHM		5% 1/4W	81349	RC07GF151J
R10	000203	RES	CARBON	20 K		5% 1/4W	81349	RC07GF203J
R11	000151	RES	CARBON	150 OHM		5% 1/4W	81349	RC07GF151J
R12	010124	RES	METAL	19.6 K	T-0	1% 1/4W	81349	RN60D1962F
R13	406524	RES	KIT, SELECTED		406524		21793	406524
R14	040098	POT	CERMET	20 OHM	62PR20		73138	62PR20
R15	011253	RES	METAL	4.75 K	T-0	1% 1/4W	81349	RN60D4751F
R16	000431	RES	CARBON	430 OHM		5% 1/4W	81349	RC07GF431J
R17	000151	RES	CARBON	150 OHM		5% 1/4W	81349	RC07GF151J
R18	000200	RES	CARBON	20 OHM		5% 1/4W	81349	RC07GF200J
R19	000361	RES	CARBON	360 OHM		5% 1/4W	81349	RC07GF361J
R20	000361	RES	CARBON	360 OHM		5% 1/4W	81349	RC07GF361J
R21	000101	RES	CARBON	100 OHM		5% 1/4W	81349	RC07GF101J
R22	000101	RES	CARBON	100 OHM		5% 1/4W	81349	RC07GF101J
R23	000201	RES	CARBON	200 OHM		5% 1/4W	81349	RC07GF201J
R24	000302	RES	CARBON	3 K		5% 1/4W	81349	RC07GF302J
R25	000301	RES	CARBON	300 OHM		5% 1/4W	81349	RC07GF301J
R26	000472	RES	CARBON	4.7 K		5% 1/4W	81349	RC07GF472J
R27	000201	RES	CARBON	200 OHM		5% 1/4W	81349	RC07GF201J
R28	000361	RES	CARBON	360 OHM		5% 1/4W	81349	RC07GF361J
R29	000101	RES	CARBON	100 OHM		5% 1/4W	81349	RC07GF101J
R30	010137	RES	METAL	100 OHM	T-0	1%	81349	RN55C1000F
R31	000751	RES	CARBON	750 OHM		5% 1/4W	81349	RC07GF751J
R32	010129	RES	METAL	5.23 K	T-0	1%	81349	RN60D5231F
R34	000361	RES	CARBON	360 OHM		5% 1/4W	81349	RC07GF361J
R35	000202	RES	CARBON	2 K		5% 1/4W	81349	RC07GF202J
R36	000361	RES	CARBON	360 OHM		5% 1/4W	81349	RC07GF361J
R37	000101	RES	CARBON	100 OHM		5% 1/4W	81349	RC07GF101J
R38	000430	RES	CARBON	43 OHM		5% 1/4W	81349	RC07GF430J

406044 – Assy., PCB, 50 MHz PREAMP DUAL

REF DES	DANA P/N	DESCRIPTION					FSC	MANU P/N
C1	100076	CAP	CERAM	20 PFD	1 KV	5%	56289	10TCCQ20
C2	130094	CAP	MICA	220 PFD	500 V	5%	72136	SCDM10-221J
C3	120029	CAP	MYLAR	.02 MFD	200 V	10%	27556	ZT2C203K
C4	100056	CAP	CERAM	8.2 PFD	1000 V	5%	56289	10TCCV82
C5	100052	CAP	CERAM	22 PFD	1000 V	5%	56289	10TCCQ22
C6	100052	CAP	CERAM	22 PFD	1000 V	5%	56289	10TCCQ22
C7	130093	CAP	MICA	200 PFD	500 V	5%	72136	SCDM10-201J
C8	130095	CAP	MICA	390 PFD	500 V	5%	72136	SCDM10-391J
C9	100009	CAP	CERAM	5 PFD		10%	71471	TCDI-1 (N750)
C10	101174	CAP	CERAM	.001 MFD	500 V	10%	71471	SCD3X5F
C11	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C12	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C13	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C14	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C15	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C16	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C17	110001	CAP	TANTA	6.8 MFD	35 V	10%	05397	T310B685K035AS
C18	100024	CAP	CERAM	.1 MFD	5815-000Y5U104Z		72982	5815-000Y5U104Z
C19	110134	CAP	TANTA	33 MFD	10 V	20%	05397	T310B336M010AS
C20	101174	CAP	CERAM	.001 MFD	500 V	10%	71471	SCD3X5F
C21	110001	CAP	TANTA	6.8 MFD	35 V	10%	05397	T310B685K035AS
C22	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C23	100057	CAP	CERAM	.1 MFD	500 V	20%	56289	5GA-P10
C101	100061	CAP	CERAM	39 PFD	1000 V	5%	56289	10TCCQ39
C102	130094	CAP	MICA	220 PFD	500 V	5%	72136	SCDM10-221J
C103	120029	CAP	MYLAR	.02 MFD	200 V	10%	27556	ZT2C203K
C104	100056	CAP	CERAM	8.2 PFD	1000 V	5%	56289	10TCCV82
C105	100052	CAP	CERAM	22 PFD	1000 V	5%	56289	10TCCQ22
C106	100052	CAP	CERAM	22 PFD	1000 V	5%	56289	10TCCQ22
C107	130093	CAP	MICA	200 PFD	500 V	5%	72136	SCDM10-201J
C108	130095	CAP	MICA	390 PFD	500 V	5%	72136	SCDM10-391J
C109	100009	CAP	CERAM	5 PFD		10%	71471	TCDI-1 (N750)
C110	101174	CAP	CERAM	.001 MFD	500 V	10%	71471	SCD3X5F
C111	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C112	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C113	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C114	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C115	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C116	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C117	110001	CAP	TANTA	6.8 MFD	35 V	10%	05397	T310B685K035AS
C118	110134	CAP	TANTA	33 MFD	10 V	20%	05397	T310B336M010AS
C119	101174	CAP	CERAM	.001 MFD	500 V	10%	71471	SCD3X5F

406044 – Assy., PCB, 50 MHz PREAMP DUAL *continued*

REF DES	DANA P/N	DESCRIPTION					FSC	MANU P/N
C120	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C123	100057	CAP	CERAM	.1 MFD	500 V	20%	56289	5GA-P10
CR1	211236	DIODE	SILICO		007		21793	211236
CR2	211083	DIODE	SILICO		018		21793	211083
CR3	211236	DIODE	SILICO		007		21793	211236
CR4	211083	DIODE	SILICO		018		21793	211083
CR101	211236	DIODE	SILICO		007		21793	211236
CR102	211083	DIODE	SILICO		018		21793	211083
CR103	211236	DIODE	SILICO		007		21793	211236
CR104	211083	DIODE	SILICO		018		21793	211083
L1	310071	CHOKE	RF	10 µH		10%	99800	1537-36
L2	310070	CHOKE	RF	5.6 µH		10%	99800	1537 Series
L3	310068	CHOKE	RF	1 µH		10%	99800	1537-12
L4	310067	CHOKE	RF	33 µH	DD-33.0		83125	DD-33.0
L5	310062	CHOKE	RF	22 µH		10%	99800	1537-44
L6	310062	CHOKE	RF	22 µH		10%	99800	1537-44
L101	310071	CHOKE	RF	10 µH		10%	99800	1537-36
L102	310070	CHOKE	RF	5.6 µH		10%	99800	1537 Series
M1	230043	INTEGRATED CIRCUIT			MC1010P		04713	MC1010P
M101	230043	INTEGRATED CIRCUIT			MC1010P		04713	MC1010P
Q1	200173	TRANS			200173		21793	200173
Q2	200099	TRANS			2N4258		81349	2N4258
Q3	200151	TRANS	SILICO		2N5179		81349	2N5179
Q4	200186	TRANS	MATCHED SET WITH Q8		200186		21793	200186
Q5	200151	TRANS	SILICO		2N5179		81349	2N5179
Q6	200151	TRANS	SILICO		2N5179		81349	2N5179
Q7	200151	TRANS	SILICO		2N5179		81349	2N5179
Q8	200186	TRANS	MATCHED SET WITH Q4		200186		21793	200186
Q9	200043	TRANS			200043		21793	200043
Q101	200173	TRANS			200173		21793	200173
Q102	200099	TRANS			2N4258		81349	2N4258
Q103	200151	TRANS	SILICO		2N5179		81349	2N5179
Q104	200186	TRANS	MATCHED SET WITH Q108		200186		21793	200186
Q105	200151	TRANS	SILICO		2N5179		81349	2N5179
Q106	200151	TRANS	SILICO		2N5179		81349	2N5179
Q107	200151	TRANS	SILICO		2N5179		81349	2N5179
Q108	200186	TRANS	MATCHED SET WITH Q104		200186		21793	200186
Q109	200043	TRANS			200043		21793	200043

406044 – Assy., PCB, 50 MHz PREAMP DUAL *continued*

REF DES	DANA P/N	DESCRIPTION					FSC	MANU P/N
R1	000106	RES	CARBON	10 M		5% 1/4W	81349	RC07GF106J
R2	010091	RES	METAL	11 K	T-0	1%	81349	RN60D1102F
R3	010329	RES	METAL	887 K	T-0	1%	81349	RN60D8873F
R4	010317	RES	METAL	90.9 K		1%	81349	RN60D9092F
R5	010317	RES	METAL	90.9 K		1%	81349	RN60D9092F
R6	010060	RES	METAL	10 K	T-0	1%	81349	RN60D1002F
R7	000203	RES	CARBON	20 K		5% 1/4W	81349	RC07GF203J
R8	000824	RES	CARBON	820 K		5% 1/4W	81349	RC07GF824J
R9	000151	RES	CARBON	150 OHM		5% 1/4W	81349	RC07GF151J
R10	000151	RES	CARBON	150 OHM		5% 1/4W	81349	RC07GF151J
R11	000203	RES	CARBON	20 K		5% 1/4W	81349	RC07GF203J
R12	010124	RES	METAL	19.6 K	T-0	1% 1/4W	81349	RN60D1962F
R13	406524	RES	KIT, SELECTED		406524		21793	406524
R14	040098	POT	CERMET	20 OHM	62PR20		73138	62PR20
R15	011253	RES	METAL	4.75 K	T-0	1% 1/4W	81349	RN60D4751F
R16	000431	RES	CARBON	430 OHM		5% 1/4W	81349	RC07GF431J
R17	000151	RES	CARBON	150 OHM		5% 1/4W	81349	RC07GF151J
R18	000200	RES	CARBON	20 OHM		5% 1/4W	81349	RC07GF200J
R19	000361	RES	CARBON	360 OHM		5% 1/4W	81349	RC07GF361J
R20	000431	RES	CARBON	430 OHM		5% 1/4W	81349	RC07GF431J
R21	000101	RES	CARBON	100 OHM		5% 1/4W	81349	RC07GF101J
R22	000101	RES	CARBON	100 OHM		5% 1/4W	81349	RC07GF101J
R23	000201	RES	CARBON	200 OHM		5% 1/4W	81349	RC07GF201J
R24	000273	RES	CARBON	27 K		5% 1/4W	81349	RC07GF273J
R25	000301	RES	CARBON	300 OHM		5% 1/4W	81349	RC07GF301J
R26	000302	RES	CARBON	3 K		5% 1/4W	81349	RC07GF302J
R27	000472	RES	CARBON	4.7 K		5% 1/4W	81349	RC07GF472J
R28	000273	RES	CARBON	27 K		5% 1/4W	81349	RC07GF273J
R29	000201	RES	CARBON	200 OHM		5% 1/4W	81349	RC07GF201J
R30	000431	RES	CARBON	430 OHM		5% 1/4W	81349	RC07GF431J
R31	000101	RES	CARBON	100 OHM		5% 1/4W	81349	RC07GF101J
R32	000333	RES	CARBON	33 K		5% 1/4W	81349	RC07GF333J
R33	000751	RES	CARBON	750 OHM		5% 1/4W	81349	RC07GF751J
R34	010137	RES	METAL	100 OHM	T-0	1%	81349	RN55C1000F
R35	000202	RES	CARBON	2 K		5% 1/4W	81349	RC07GF202J
R36	010129	RES	METAL	5.23 K	T-0	1%	81349	RN60D5231F
R38	000361	RES	CARBON	360 OHM		5% 1/4W	81349	RC07GF361J
R39	000100	RES	CARBON	10 OHM		5% 1/4W	81349	RC07GF100J
R40	000361	RES	CARBON	360 OHM		5% 1/4W	81349	RC07GF361J
R41	000103	RES	CARBON	10 K		5% 1/4W	81349	RC07GF103J
R42	000102	RES	CARBON	1 K		5% 1/4W	81349	RC07GF102J
R43	000392	RES	CARBON	3.9 K		5% 1/4W	81349	RC07GF392J

406044 – Assy., PCB, 50 MHz PREAMP DUAL *continued*

REF DES	DANA P/N	DESCRIPTION					FSC	MANU P/N
R44	000750	RES	CARBON	75 OHM		5% 1/4W	81349	RC07GF750J
R45	000105	RES	CARBON	1 M		5% 1/4W	81349	RC07GF105J
R46	000101	RES	CARBON	100 OHM		5% 1/4W	81349	RC07GF101J
R47	000430	RES	CARBON	43 OHM		5% 1/4W	81349	RC07GF430J
R101	000106	RES	CARBON	10 M		5% 1/4W	81349	RC07GF106J
R102	010091	RES	METAL	11 K	T-0	1%	81349	RN60D1102F
R103	010329	RES	METAL	887 K	T-0	1%	81349	RN60D8873F
R104	010317	RES	METAL	90.9 K		1%	81349	RN60D9092F
R105	010317	RES	METAL	90.9 K		1%	81349	RN60D9092F
R106	010060	RES	METAL	10 K	T-0	1%	81349	RN60D1002F
R107	000203	RES	CARBON	20 K		5% 1/4W	81349	RC07GF203J
R108	000824	RES	CARBON	820 K		5% 1/4W	81349	RC07GF824J
R109	000151	RES	CARBON	150 OHM		5% 1/4W	81349	RC07GF151J
R110	000151	RES	CARBON	150 OHM		5% 1/4W	81349	RC07GF151J
R111	000203	RES	CARBON	20 K		5% 1/4W	81349	RC07GF203J
R112	010124	RES	METAL	19.6 K	T-0	1% 1/4W	81349	RN60D1962F
R113	406524	RES	KIT, SELECTED		406524		21793	406524
R114	040098	POT	CERMET	20 OHM	62PR20		73138	62PR20
R115	011253	RES	METAL	4.75 K	T-0	1% 1/4W	81349	RN60D4751F
R116	000431	RES	CARBON	430 OHM		5% 1/4W	81349	RC07GF431J
R117	000151	RES	CARBON	150 OHM		5% 1/4W	81349	RC07GF151J
R118	000200	RES	CARBON	20 OHM		5% 1/4W	81349	RC07GF200J
R119	000361	RES	CARBON	360 OHM		5% 1/4W	81349	RC07GF361J
R120	000431	RES	CARBON	430 OHM		5% 1/4W	81349	RC07GF431J
R121	000101	RES	CARBON	100 OHM		5% 1/4W	81349	RC07GF101J
R122	000101	RES	CARBON	100 OHM		5% 1/4W	81349	RC07GF101J
R123	000201	RES	CARBON	200 OHM		5% 1/4W	81349	RC07GF201J
R124	000301	RES	CARBON	300 OHM		5% 1/4W	81349	RC07GF301J
R125	000302	RES	CARBON	3 K		5% 1/4W	81349	RC07GF302J
R126	000472	RES	CARBON	4.7 K		5% 1/4W	81349	RC07GF472J
R127	000201	RES	CARBON	200 OHM		5% 1/4W	81349	RC07GF201J
R128	000431	RES	CARBON	430 OHM		5% 1/4W	81349	RC07GF431J
R129	000101	RES	CARBON	100 OHM		5% 1/4W	81349	RC07GF101J
R130	000333	RES	CARBON	33 K		5% 1/4W	81349	RC07GF333J
R131	010137	RES	METAL	100 OHM	T-0	1%	81349	RN55C1000F
R132	000751	RES	CARBON	750 OHM		5% 1/4W	81349	RC07GF751J
R133	010129	RES	METAL	5.23 K	T-0	1%	81349	RN60D5231F
R135	000202	RES	CARBON	2 K		5% 1/4W	81349	RC07GF202J
R136	000361	RES	CARBON	360 OHM		5% 1/4W	81349	RC07GF361J
R137	000100	RES	CARBON	10 OHM		5% 1/4W	81349	RC07GF100J
R138	000101	RES	CARBON	100 OHM		5% 1/4W	81349	RC07GF101J
R139	000103	RES	CARBON	10 K		5% 1/4W	81349	RC07GF103J

406044 – Assy., PCB, 50 MHz PREAMP DUAL *continued*

REF DES	DANA P/N	DESCRIPTION				FSC	MANU P/N
R140	000102	RES	CARBON	1 K	5% 1/4W	81349	RC07GF102J
R141	000392	RES	CARBON	3.9 K	5% 1/4W	81349	RC07GF392J
R142	000750	RES	CARBON	75 OHM	5% 1/4W	81349	RC07GF750J
R143	000105	RES	CARBON	1 M	5% 1/4W	81349	RC07GF105J
R144	000430	RES	CARBON	43 OHM	5% 1/4W	81349	RC07GF430J

406048 – Assy., PCB, 500 MHz PRESCALER

REF DES	DANA P/N	DESCRIPTION					FSC	MANU P/N
C1	130104	CAP	CERAM	1000 PFD	100 V	20%	72982	9ACF-W5R102M
C2	110022	CAP	TANTA	3.3 MFD	35 V	10%	05397	T310B335K035AS
C3	130104	CAP	CERAM	1000 PFD	100 V	20%	72982	9ACF-W5R102M
C4	130104	CAP	CERAM	1000 PFD	100 V	20%	72982	9ACF-W5R102M
C5	130103	CAP	CERAM	10000 PFD	25 V	20%	72982	9ACF-W5R103M
C6	130103	CAP	CERAM	10000 PFD	25 V	20%	72982	9ACF-W5R103M
C7	130104	CAP	CERAM	1000 PFD	100 V	20%	72982	9ACF-W5R102M
C8	130103	CAP	CERAM	10000 PFD	25 V	20%	72982	9ACF-W5R103M
C9	130104	CAP	CERAM	1000 PFD	100 V	20%	72982	9ACF-W5R102M
C10	130104	CAP	CERAM	1000 PFD	100 V	20%	72982	9ACF-W5R102M
C11	130103	CAP	CERAM	10000 PFD	25 V	20%	72982	9ACF-W5R103M
C12	130103	CAP	CERAM	10000 PFD	25 V	20%	72982	9ACF-W5R103M
C13	130104	CAP	CERAM	1000 PFD	100 V	20%	72982	9ACF-W5R102M
C14	130104	CAP	CERAM	1000 PFD	100 V	20%	72982	9ACF-W5R102M
C15	130104	CAP	CERAM	1000 PFD	100 V	20%	72982	9ACF-W5R102M
C16	130103	CAP	CERAM	10000 PFD	25 V	20%	72982	9ACF-W5R103M
C17	101174	CAP	CERAM	.001 MFD	500 V	10%	71471	SCD3X5F
C18	130105	CAP	CERAM	500 PFD		20%	72982	9ACF-C0G501M
C19	101174	CAP	CERAM	.001 MFD	500 V	10%	71471	SCD3X5F
C20	130104	CAP	CERAM	1000 PFD	100 V	20%	72982	9ACF-W5R102M
C21	130106	CAP	CERAM	120 PFD	25 V	20%	72982	9ACF-C0G121M
C22	101174	CAP	CERAM	.001 MFD	500 V	10%	71471	SCD3X5F
C23	101174	CAP	CERAM	.001 MFD	500 V	10%	71471	SCD3X5F
C24	130104	CAP	CERAM	1000 PFD	100 V	20%	72982	9ACF-W5R102M
C25	130106	CAP	CERAM	120 PFD	25 V	20%	72982	9ACF-C0G121M
C26	101174	CAP	CERAM	.001 MFD	500 V	10%	71471	SCD3X5F
C27	101174	CAP	CERAM	.001 MFD	500 V	10%	71471	SCD3X5F
C28	110022	CAP	TANTA	3.3 MFD	35 V	10%	05397	T310B335K035AS
C29	130104	CAP	CERAM	1000 PFD	100 V	20%	72982	9ACF-W5R102M
C30	130106	CAP	CERAM	120 PFD	25 V	20%	72982	9ACF-C0G121M
C31	101174	CAP	CERAM	.001 MFD	500 V	10%	71471	SCD3X5F
C32	101174	CAP	CERAM	.001 MFD	500 V	10%	71471	SCD3X5F
C34	130103	CAP	CERAM	10000 PFD	25 V	20%	72982	9ACF-W5R103M
C35	130104	CAP	CERAM	1000 PFD	100 V	20%	72982	9ACF-W5R102M
C36	130104	CAP	CERAM	1000 PFD	100 V	20%	72982	9ACF-W5R102M
C38	130105	CAP	CERAM	500 PFD		20%	72982	9ACF-C0G501M
C40	130103	CAP	CERAM	10000 PFD	25 V	20%	72982	9ACF-W5R103M

406048 – Assy., PCB, 500 MHz PRESCALER *continued*

REF DES	DANA P/N	DESCRIPTION					FSC	MANU P/N
C42	101174	CAP	CERAM	.001 MFD	500 V	10%	71471	SCD3X5F
C43	101174	CAP	CERAM	.001 MFD	500 V	10%	71471	SCD3X5F
C44	130104	CAP	CERAM	1000 PFD	100 V	20%	72982	9ACF-W5R102M
C46	101174	CAP	CERAM	.001 MFD	500 V	10%	71471	SCD3X5F
C47	101174	CAP	CERAM	.001 MFD	500 V	10%	71471	SCD3X5F
C48	101174	CAP	CERAM	.001 MFD	500 V	10%	71471	SCD3X5F
C49	101174	CAP	CERAM	.001 MFD	500 V	10%	71471	SCD3X5F
C50	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C51	110022	CAP	TANTA	3.3 MFD	35 V	10%	05397	T310B335K035AS
C52	110022	CAP	TANTA	3.3 MFD	35 V	10%	05397	T310B335K035AS
C53	100014	CAP	CERAM	910 PFD	1000 V	10%	71471	GPDX5F911K
C54	100043	CAP	CERAM	.003 MFD	1000 V	10%	71590	DD302
C55	110022	CAP	TANTA	3.3 MFD	35 V	10%	05397	T310B335K035AS
C56	110022	CAP	TANTA	3.3 MFD	35 V	10%	05397	T310B335K035AS
C57	110022	CAP	TANTA	3.3 MFD	35 V	10%	05397	T310B335K035AS
C58	130121	CAP	CHIP	10 MFD	100 V		72982	8013-201-100
C59	101174	CAP	CERAM	.001 MFD	500 V	10%	71471	SCD3X5F
C60	101174	CAP	CERAM	.001 MFD	500 V	10%	71471	SCD3X5F
C61	130104	CAP	CERAM	1000 PFD	100 V	20%	72982	9ACF-W5R102M
C62	101174	CAP	CERAM	.001 MFD	500 V	10%	71471	SCD3X5F
C63	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C64	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C65	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C66	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C67	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C68	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C69	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C70	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C71	130104	CAP	CERAM	1000 PFD	100 V	20%	72982	9ACF-W5R102M
C72	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C73	130103	CAP	CERAM	10000 PFD	25 V	20%	72982	9ACF-W5R103M
CR1	210022	DIODE			HP5082-3080		50434	HP5082-3080
CR2	220007	DIODE	SILICO	ZENER	1N751A		81349	1N751A
CR3	220007	DIODE	SILICO	ZENER	1N751A		81349	1N751A
CR4	210022	DIODE			HP5082-3080		50434	HP5082-3080
CR5	210022	DIODE			HP5082-3080		50434	HP5082-3080
CR6	210022	DIODE			HP5082-3080		50434	HP5082-3080
CR7	210014	DIODE			1N4005		81349	1N4005
CR8	210022	DIODE			HP5082-3080		50434	HP5082-3080
CR9	210026	DIODE	RF DET		1N82AG		81349	1N82AG
CR10	210026	DIODE	RF DET		1N82AG		81349	1N82AG

406048 – Assy., PCB, 500 MHz PRESCALER *continued*

REF DES	DANA P/N	DESCRIPTION	FSC	MANU P/N
CR11	211083	DIODE SILICO 018	21793	211083
CR12	211083	DIODE SILICO 018	21793	211083
CR13	211083	DIODE SILICO 018	21793	211083
CR14	211083	DIODE SILICO 018	21793	211083
CR15	211083	DIODE SILICO 018	21793	211083
CR16	210030	DIODE TD253A		TD253A
CR17	210015	DIODE HP5082-2800	50434	HP5082-2800
CR18	210019	DIODE MATCHED SET 210019	21793	210019
CR19	210019	DIODE MATCHED SET 210019	21793	210019
CR20	220007	DIODE SILICO ZENER 1N751A	81349	1N751A
J12	600573	CONN RF 50-051-0000	98291	50-051-0000
L1	406464	CHOKE ASSY 406464	21793	406464
L2	310083	CHOKE 24 GA 310083	21793	310083
L3	310084	CHOKE 24 GA 310084	21793	310084
L4	406464	CHOKE ASSY 406464	21793	406464
L5	310082	CHOKE 24 GA 310082	21793	310082
L6	310084	CHOKE 24 GA 310084	21793	310084
L7	406464	CHOKE ASSY 406464	21793	406464
L8	310082	CHOKE 24 GA 310082	21793	310082
L9	310084	CHOKE 24 GA 310084	21793	310084
L10	406464	CHOKE ASSY 406464	21793	406464
L11	310082	CHOKE 24 GA 310082	21793	310082
L12	310084	CHOKE 24 GA 310084	21793	310084
L15	406481	CHOKE ASSY 406481	21793	406481
L16	310083	CHOKE 24 GA 310083	21793	310083
L17	310084	CHOKE 24 GA 310084	21793	310084
L19	406496	CHOKE ASSY 406496	21793	406496
L20	310081	CHOKE 24 GA 310081	21793	310081
M1	230062	INTEGRATED CIRCUIT SN7400N	01295	SN7400N
M2	230045	INTEGRATED CIRCUIT μA741C	07263	U6E7741393
M3	230045	INTEGRATED CIRCUIT μA741C	07263	U6E7741393
M4	230083	INTEGRATED CIRCUIT MC1670S	04713	MC1670S
M5	230083	INTEGRATED CIRCUIT MC1670S	04713	MC1670S
M6	230083	INTEGRATED CIRCUIT MC1670S	04713	MC1670S
Q1	200153	TRANS SILICO NPN K2122A	20754	K2122A
Q2	200153	TRANS SILICO NPN K2122A	20754	K2122A
Q3	200153	TRANS SILICO NPN K2122A	20754	K2122A
Q4	200153	TRANS SILICO NPN K2122A	20754	K2122A

406048 – Assy., PCB, 500 MHz PRESCALER *continued*

REF DES	DANA P/N	DESCRIPTION	FSC	MANU P/N
Q6	200156	TRANS SILICO NPN K2063	20754	K2063
Q7	200088	TRANS SILICO PNP 2N4248	80131	2N4248
Q8	200149	TRANS SILICO NPN 2N3569	81349	2N3569
Q9	200148	TRANS SILICO PNP 2N3638	81349	2N3638
Q10	200151	TRANS SILICO 2N5179	81349	2N5179
Q11	200151	TRANS SILICO 2N5179	81349	2N5179
Q12	200151	TRANS SILICO 2N5179	81349	2N5179
R1	000101	RES CARBON 100 OHM 5% 1/4W	81349	RC07GF101J
R2	001683	RES CARBON 47 OHM 5% 1/2W	81349	RC20GF470J
R3	001684	RES CARBON 39 OHM 5% 1/2W	81349	RC20GF390F
R4	000100	RES CARBON 10 OHM 5% 1/4W	81349	RC07GF100J
R5	000100	RES CARBON 10 OHM 5% 1/4W	81349	RC07GF100J
R6	001472	RES CARBON 10 OHM 5% 1/2W	81349	RC20GF100J
R7	000362	RES CARBON 3.6 K 5% 1/4W	81349	RC07GF362J
R8	000100	RES CARBON 10 OHM 5% 1/4W	81349	RC07GF100J
R9	001159	RES CARBON 330 OHM 5% 1/4W	81349	RC20GF331J
R10	000101	RES CARBON 100 OHM 5% 1/4W	81349	RC07GF101J
R11	000470	RES CARBON 47 OHM 5% 1/4W	81349	RC07GF470J
R12	001773	RES CARBON 200 OHM 5% 1/8W	81349	RC07GF201J
R13	000822	RES CARBON 8.2 K 5% 1/4W	81349	RC07GF822J
R14	000203	RES CARBON 20 K 5% 1/4W	81349	RC07GF203J
R15	000132	RES CARBON 1.3 K 5% 1/4W	81349	RC07GF132J
R16	000100	RES CARBON 10 OHM 5% 1/4W	81349	RC07GF100J
R17	000203	RES CARBON 20 K 5% 1/4W	81349	RC07GF203J
R18	001773	RES CARBON 200 OHM 5% 1/8W	81349	RC07GF201J
R19	000822	RES CARBON 8.2 K 5% 1/4W	81349	RC07GF822J
R20	000132	RES CARBON 1.3 K 5% 1/4W	81349	RC07GF132J
R21	000100	RES CARBON 10 OHM 5% 1/4W	81349	RC07GF100J
R22	000203	RES CARBON 20 K 5% 1/4W	81349	RC07GF203J
R23	001773	RES CARBON 200 OHM 5% 1/8W	81349	RC07GF201J
R24	000822	RES CARBON 8.2 K 5% 1/4W	81349	RC07GF822J
R25	000132	RES CARBON 1.3 K 5% 1/4W	81349	RC07GF132J
R26	000100	RES CARBON 10 OHM 5% 1/4W	81349	RC07GF100J
R27	000203	RES CARBON 20 K 5% 1/4W	81349	RC07GF203J
R28	001773	RES CARBON 200 OHM 5% 1/8W	81349	RC07GF201J
R29	000822	RES CARBON 8.2 K 5% 1/4W	81349	RC07GF822J
R30	000132	RES CARBON 1.3 K 5% 1/4W	81349	RC07GF132J
R31	000100	RES CARBON 10 OHM 5% 1/4W	81349	RC07GF100J
R34	000153	RES CARBON 15 K 5% 1/4W	81349	RC07GF153J
R36	001773	RES CARBON 200 OHM 5% 1/8W	81349	RC07GF201J
R37	000822	RES CARBON 8.2 K 5% 1/4W	81349	RC07GF822J

406048 – Assy., PCB, 500 MHz PRESCALER *continued*

REF DES	DANA P/N	DESCRIPTION					FSC	MANU P/N
R38	000561	RES	CARBON	560 OHM		5% 1/4W	81349	RC07GF561J
R39	000100	RES	CARBON	10 OHM		5% 1/4W	81349	RC07GF100J
R40	000100	RES	CARBON	10 OHM		5% 1/4W	81349	RC07GF100J
R41	000132	RES	CARBON	1.3 K		5% 1/4W	81349	RC07GF132J
R42	000102	RES	CARBON	1 K		5% 1/4W	81349	RC07GF102J
R43	000472	RES	CARBON	4.7 K		5% 1/4W	81349	RC07GF472J
R44	000202	RES	CARBON	2 K		5% 1/4W	81349	RC07GF202J
R45	000472	RES	CARBON	4.7 K		5% 1/4W	81349	RC07GF472J
R46	000822	RES	CARBON	8.2 K		5% 1/4W	81349	RC07GF822J
R47	000680	RES	CARBON	68 OHM		5% 1/4W	81349	RC07GF680J
R48	000430	RES	CARBON	43 OHM		5% 1/4W	81349	RC07GF430J
R49	000101	RES	CARBON	100 OHM		5% 1/4W	81349	RC07GF101J
R50	000150	RES	CARBON	15 OHM		5% 1/4W	81349	RC07GF150J
R51	000302	RES	CARBON	3 K		5% 1/4W	81349	RC07GF302J
R52	001770	RES	CARBON	150 OHM		5% 1 W		
R53	000822	RES	CARBON	8.2 K		5% 1/4W	81349	RC07GF822J
R54	000111	RES	CARBON	110 OHM		5% 1/4W	81349	RC07GF111J
R55	000201	RES	CARBON	200 OHM		5% 1/4W	81349	RC07GF201J
R56	000362	RES	CARBON	3.6 K		5% 1/4W	81349	RC07GF362J
R57	000100	RES	CARBON	10 OHM		5% 1/4W	81349	RC07GF100J
R58	000100	RES	CARBON	10 OHM		5% 1/4W	81349	RC07GF100J
R59	000181	RES	CARBON	180 OHM		5% 1/4W	81349	RC07GF181J
R60	000302	RES	CARBON	3 K		5% 1/4W	81349	RC07GF302J
R61	000104	RES	CARBON	100 K		5% 1/4W	81349	RC07GF104J
R62	000512	RES	CARBON	5.1 K		5% 1/4W	81349	RC07GF512J
R63	000272	RES	CARBON	2.7 K		5% 1/4W	81349	RC07GF272J
R64	040123	POT	CERMET	1 K	62-1-1-102		73138	62-1-1-102
R65	000392	RES	CARBON	3.9 K		5% 1/4W	81349	RC07GF392J
R66	000512	RES	CARBON	5.1 K		5% 1/4W	81349	RC07GF512J
R67	000512	RES	CARBON	5.1 K		5% 1/4W	81349	RC07GF512J
R68	000103	RES	CARBON	10 K		5% 1/4W	81349	RC07GF103J
R69	000101	RES	CARBON	100 OHM		5% 1/4W	81349	RC07GF101J
R70	000750	RES	CARBON	75 OHM		5% 1/4W	81349	RC07GF750J
R71	040123	POT	CERMET	1 K	62-1-1-102		73138	62-1-1-102
R72	000182	RES	CARBON	1.8 K		5% 1/4W	81349	RC07GF182J
R73	000331	RES	CARBON	330 OHM		5% 1/4W	81349	RC07GF331J
R74	000130	RES	CARBON	13 OHM		5% 1/4W	81349	RC07GF130J
R75	000302	RES	CARBON	3 K		5% 1/4W	81349	RC07GF302J
R76	000360	RES	CARBON	36 OHM		5% 1/4W	81349	RC07GF360J
R77	000511	RES	CARBON	510 OHM		5% 1/4W	81349	RC07GF511J
R78	000510	RES	CARBON	51 OHM		5% 1/4W	81349	RC07GF510J
R79	040123	POT	CERMET	1 K	62-1-1-102		73138	62-1-1-102

406048 – Assy., PCB, 500 MHz PRESCALER *continued*

REF DES	DANA P/N	DESCRIPTION					FSC	MANU P/N
R80	000102	RES	CARBON	1 K		5% 1/4W	81349	RC07GF102J
R81	000620	RES	CARBON	62 OHM		5% 1/4W	81349	RC07GF620J
R82	000620	RES	CARBON	62 OHM		5% 1/4W	81349	RC07GF620J
R83	000151	RES	CARBON	150 OHM		5% 1/4W	81349	RC07GF151J
R84	000151	RES	CARBON	150 OHM		5% 1/4W	81349	RC07GF151J
R85	000101	RES	CARBON	100 OHM		5% 1/4W	81349	RC07GF101J
R86	000511	RES	CARBON	510 OHM		5% 1/4W	81349	RC07GF511J
R87	000511	RES	CARBON	510 OHM		5% 1/4W	81349	RC07GF511J
R88	000511	RES	CARBON	510 OHM		5% 1/4W	81349	RC07GF511J
R89	000511	RES	CARBON	510 OHM		5% 1/4W	81349	RC07GF511J
R90	000511	RES	CARBON	510 OHM		5% 1/4W	81349	RC07GF511J
R91	000241	RES	CARBON	240 OHM		5% 1/4W	81349	RC07GF241J
R92	000131	RES	CARBON	130 OHM		5% 1/4W	81349	RC07GF131J
R93	000200	RES	CARBON	20 OHM		5% 1/4W	81349	RC07GF200J
R94	000472	RES	CARBON	4.7 K		5% 1/4W	81349	RC07GF472J
R95	000202	RES	CARBON	2 K		5% 1/4W	81349	RC07GF202J
R96	000510	RES	CARBON	51 OHM		5% 1/4W	81349	RC07GF510J
R97	000300	RES	CARBON	30 OHM		5% 1/4W	81349	RC07GF300J
R98	000680	RES	CARBON	68 OHM		5% 1/4W	81349	RC07GF680J
R99	000511	RES	CARBON	510 OHM		5% 1/4W	81349	RC07GF511J
RFC1	310055	CHOKE	RF	4.7 µH	9310-28		76493	9310-28
RFC2	310055	CHOKE	RF	4.7 µH	9310-28		76493	9310-28
RFC3	310072	CHOKE	RF	2.2 µH		10%	99800	1537-20
RFC4	310055	CHOKE	RF	4.7 µH	9310-28		76493	9310-28
RFC5	310055	CHOKE	RF	4.7 µH	9310-28		76493	9310-28
RFC6	310055	CHOKE	RF	4.7 µH	9310-28		76493	9310-28
RFC7	310072	CHOKE	RF	2.2 µH		10%	99800	1537-20
RFC8	310072	CHOKE	RF	2.2 µH		10%	99800	1537-20
RFC9	310056	CHOKE	RF	.68 µH	9230-16		76493	9230-16
RFC10	310056	CHOKE	RF	.68 µH	9230-16		76493	9230-16
RFC11	310056	CHOKE	RF	.68 µH	9230-16		76493	9230-16
RFC12	310056	CHOKE	RF	.68 µH	9230-16		76493	9230-16
RFC13	310056	CHOKE	RF	.68 µH	9230-16		76493	9230-16
RFC14	310056	CHOKE	RF	.68 µH	9230-16		76493	9230-16
RFC15	310056	CHOKE	RF	.68 µH	9230-16		76493	9230-16
RFC16	310056	CHOKE	RF	.68 µH	9230-16		76493	9230-16
RFC17	310056	CHOKE	RF	.68 µH	9230-16		76493	9230-16
RFC18	310072	CHOKE	RF	2.2 µH		10%	99800	1537-20
RFC19	310072	CHOKE	RF	2.2 µH		10%	99800	1537-20
RFC20	310072	CHOKE	RF	2.2 µH		10%	99800	1537-20

406048 – Assy., PCB, 500 MHz PRESCALER *continued*

REF DES	DANA P/N	DESCRIPTION					FSC	MANU P/N
RFC21	310072	CHOKE	RF	2.2 μH		10%	99800	1537-20
RFC22	406466	CHOKE	ASSY		406466		21793	406466
RFC23	406466	CHOKE	ASSY		406466		21793	406466
RFC24	406466	CHOKE	ASSY		406466		21793	406466
RFC25	310056	CHOKE	RF	.68 μH	9230-16		76493	9230-16
RFC26	310056	CHOKE	RF	.68 μH	9230-16		76493	9230-16
RFC27	406466	CHOKE	ASSY		406466		21793	406466
RFC28	406466	CHOKE	ASSY		406466		21793	406466
RFC29	406466	CHOKE	ASSY		406466		21793	406466
RFC30	406466	CHOKE	ASSY		406466		21793	406466
RFC31	406466	CHOKE	ASSY		406466		21793	406466
RFC32	406466	CHOKE	ASSY		406466		21793	406466
RFC33	406466	CHOKE	ASSY		406466		21793	406466

406047 – Assy., PCB, PROGRAM SIGNAL CONDITIONER – SINGLE

REF DES	DANA P/N	DESCRIPTION					FSC	MANU P/N
C1	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C2	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C3	110134	CAP	TANTA	33 MFD	10 V	20%	05397	T310B336M010AS
C4	110001	CAP	TANTA	6.8 MFD	35 V	10%	05397	T310B685K035AS
C5	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C6	110001	CAP	TANTA	6.8 MFD	35 V	10%	05397	T310B685K035AS
C101	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C102	100009	CAP	CERAM	5 PFD		10%	71471	TCDI-1 (N750)
C103	100057	CAP	CERAM	.1 MFD	500 V	20%	56289	5GA-P10
C104	100041	CAP	CERAM	25 PFD	1000 V	5%	56289	10TCCQ25
C105	130065	CAP	MICA	330 PFD	500 V	5%	09023	C015FD331J03
C106	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C107	130066	CAP	MICA	100 PFD	500 V	5%	09023	C015FD101J03
C108	130083	CAP	MICA	750 PFD	CM06FD751J03		72136	CM06FD751J03
C109	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C110	130076	CAP	MICA	200 PFD	500 V	5%	72136	DM15-201J
C111	130091	CAP	MICA	.0016 MFD	500 V	5%	72136	CM06F162J03
C112	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C113	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C114	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C115	101174	CAP	CERAM	.001 MFD	500 V	10%	71471	SCD3X5F
C116	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C117	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C118	100024	CAP	CERAM	.1 MFD	5815-000Y5U104Z		72982	5815-000Y5U104Z
C119	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C120	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C121	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C122	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C123	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C124	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C125	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
CR101	211083	DIODE	SILICO		018		21793	211083
CR102	211083	DIODE	SILICO		018		21793	211083
CR103	211236	DIODE	SILICO		007		21793	211236
CR104	211236	DIODE	SILICO		007		21793	211236
CR105	211236	DIODE	SILICO		007		21793	211236
CR106	211236	DIODE	SILICO		007		21793	211236
CR107	210013	DIODE	SILICO		1N916		81349	1N916
CR108	210013	DIODE	SILICO		1N916		81349	1N916
CR109	210013	DIODE	SILICO		1N916		81349	1N916
CR110	210013	DIODE	SILICO		1N916		81349	1N916

406047 – Assy., PCB, PROGRAM SIGNAL CONDITIONER – SINGLE *continued*

REF DES	DANA P/N	DESCRIPTION	FSC	MANU P/N
CR111	210013	DIODE SILICO 1N916	81349	1N916
CR112	210013	DIODE SILICO 1N916	81349	1N916
CR113	211083	DIODE SILICO 018	21793	211083
CR114	211083	DIODE SILICO 018	21793	211083
CR115	211083	DIODE SILICO 018	21793	211083
CR116	211083	DIODE SILICO 018	21793	211083
CR117	211083	DIODE SILICO 018	21793	211083
CR118	211083	DIODE SILICO 018	21793	211083
CR119	211083	DIODE SILICO 018	21793	211083
CR120	211083	DIODE SILICO 018	21793	211083
CR121	211083	DIODE SILICO 018	21793	211083
CR122	211083	DIODE SILICO 018	21793	211083
CR123	211083	DIODE SILICO 018	21793	211083
CR124	211083	DIODE SILICO 018	21793	211083
CR125	211083	DIODE SILICO 018	21793	211083
CR126	211083	DIODE SILICO 018	21793	211083
CR127	211083	DIODE SILICO 018	21793	211083
CR128	211083	DIODE SILICO 018	21793	211083
CR129	211083	DIODE SILICO 018	21793	211083
CR130	220031	DIODE SILICO ZENER 1/4M3.3AZ5	04713	1/4M3.3AZ5
CR131	220031	DIODE SILICO ZENER 1/4M3.3AZ5	04713	1/4M3.3AZ5
L1	310062	CHOKE RF 22 µH 10%	99800	1537-44
L2	310062	CHOKE RF 22 µH 10%	99800	1537-44
L3	310070	CHOKE RF 5.6 µH 10%	99800	1537 Series
L4	310062	CHOKE RF 22 µH 10%	99800	1537-44
L5	310062	CHOKE RF 22 µH 10%	99800	1537-44
L101	310070	CHOKE RF 5.6 µH 10%	99800	1537 Series
L102	310068	CHOKE RF 1 µH 10%	99800	1537-12
M1	230069	INTEGRATED CIRCUIT MC4007	04713	MC4007
M2	230028	INTEGRATED CIRCUIT SN7400N	01295	SN7400N
M3	230028	INTEGRATED CIRCUIT SN7400N	01295	SN7400N
M4	230028	INTEGRATED CIRCUIT SN7400N	01295	SN7400N
M5	230028	INTEGRATED CIRCUIT SN7400N	01295	SN7400N
M6	230028	INTEGRATED CIRCUIT SN7400N	01295	SN7400N
M101	230028	INTEGRATED CIRCUIT SN7400N	01295	SN7400N
M102	230031	INTEGRATED CIRCUIT SN7410N	01295	SN7410N
M103	230043	INTEGRATED CIRCUIT MC1010P	04713	MC1010P
M104	230045	INTEGRATED CIRCUIT µA741C	07263	U6E7741393
M105	230028	INTEGRATED CIRCUIT SN7400N	01295	SN7400N

406047 – Assy., PCB, PROGRAM SIGNAL CONDITIONER – SINGLE *continued*

REF DES	DANA P/N	DESCRIPTION					FSC	MANU P/N
Q101	200068	TRANS			2N4250		80131	2N4250
Q102	200068	TRANS			2N4250		80131	2N4250
Q103	200173	TRANS			200173		21793	200173
Q104	200173	TRANS			200173		21793	200173
Q105	200173	TRANS			200173		21793	200173
Q106	200173	TRANS			200173		21793	200173
Q107	200173	TRANS			200173		21793	200173
Q108	200068	TRANS			2N4250		80131	2N4250
Q109	200068	TRANS			2N4250		80131	2N4250
Q110	200068	TRANS			2N4250		80131	2N4250
Q111	200043	TRANS			200043		21793	200043
Q112	200173	TRANS			200173		21793	200173
Q113	200099	TRANS			2N4258		81349	2N4258
Q114	200151	TRANS	SILICO		2N5179		81349	2N5179
Q115	200151	TRANS	SILICO		2N5179		81349	2N5179
Q116	200151	TRANS	SILICO		2N5179		81349	2N5179
Q117	200151	TRANS	SILICO		2N5179		81349	2N5179
Q118	200151	TRANS	SILICO		2N5179		81349	2N5179
Q119	200151	TRANS	SILICO		2N5179		81349	2N5179
Q120	200082	TRANS			2N4424		81349	2N4424
Q121	200082	TRANS			2N4424		81349	2N4424
Q122	200082	TRANS			2N4424		81349	2N4424
Q123	200043	TRANS			200043		21793	200043
Q124	200043	TRANS			200043		21793	200043
Q125	200043	TRANS			200043		21793	200043
Q126	200043	TRANS			200043		21793	200043
Q127	200043	TRANS			200043		21793	200043
R1	000202	RES	CARBON	2 K		5% 1/4W	81349	RC07GF202J
R2	000202	RES	CARBON	2 K		5% 1/4W	81349	RC07GF202J
R3	000202	RES	CARBON	2 K		5% 1/4W	81349	RC07GF202J
R4	000202	RES	CARBON	2 K		5% 1/4W	81349	RC07GF202J
R5	000202	RES	CARBON	2 K		5% 1/4W	81349	RC07GF202J
R6	000202	RES	CARBON	2 K		5% 1/4W	81349	RC07GF202J
R7	000202	RES	CARBON	2 K		5% 1/4W	81349	RC07GF202J
R101	000203	RES	CARBON	20 K		5% 1/4W	81349	RC07GF203J
R102	000151	RES	CARBON	150 OHM		5% 1/4W	81349	RC07GF151J
R103	000203	RES	CARBON	20 K		5% 1/4W	81349	RC07GF203J
R104	010496	RES	METAL	1 M	T-0	1% 1/8W	81349	RN60D
R105	010496	RES	METAL	1 M	T-0	1% 1/8W	81349	RN60D
R106	000202	RES	CARBON	2 K		5% 1/4W	81349	RC07GF202J
R107	000102	RES	CARBON	1 K		5% 1/4W	81349	RC07GF102J

406047 – Assy., PCB, PROGRAM SIGNAL CONDITIONER – SINGLE *continued*

REF DES	DANA P/N	DESCRIPTION					FSC	MANU P/N
R108	000102	RES	CARBON	1 K		5% 1/4W	81349	RC07GF102J
R109	000103	RES	CARBON	10 K		5% 1/4W	81349	RC07GF103J
R110	000153	RES	CARBON	15 K		5% 1/4W	81349	RC07GF153J
R111	000153	RES	CARBON	15 K		5% 1/4W	81349	RC07GF153J
R112	000153	RES	CARBON	15 K		5% 1/4W	81349	RC07GF153J
R113	000153	RES	CARBON	15 K		5% 1/4W	81349	RC07GF153J
R114	010376	RES	METAL	60.4 K	T-0	1%	81349	RN60D6042F
R115	010513	RES	METAL	6.65 K		1% 1/4W	81349	RN60D6651F
R116	010287	RES	METAL	3.01 K	T-0	1%	81349	RN60D3011F
R117	010414	RES	METAL	825 OHM		1%	81349	RN60D8250F
R118	000135	RES	CARBON	1.3 M		5% 1/4W	81349	RC07GF135J
R119	000105	RES	CARBON	1 M		5% 1/4W	81349	RC07GF105J
R120	010124	RES	METAL	19.6 K	T-0	1% 1/4W	81349	RN60D1962F
R121	406524	RES	KIT, SELECTED		406524		21793	406524
R122	040098	POT	CERMET	20 OHM	62PR20		73138	62PR20
R123	011253	RES	METAL	4.75 K	T-0	1% 1/4W	81349	RN60D4751F
R124	000431	RES	CARBON	430 OHM		5% 1/4W	81349	RC07GF431J
R125	000100	RES	CARBON	10 OHM		5% 1/4W	81349	RC07GF100J
R126	000361	RES	CARBON	360 OHM		5% 1/4W	81349	RC07GF361J
R127	000101	RES	CARBON	100 OHM		5% 1/4W	81349	RC07GF101J
R128	000302	RES	CARBON	3 K		5% 1/4W	81349	RC07GF302J
R129	000201	RES	CARBON	200 OHM		5% 1/4W	81349	RC07GF201J
R130	000273	RES	CARBON	27 K		5% 1/4W	81349	RC07GF273J
R131	000201	RES	CARBON	200 OHM		5% 1/4W	81349	RC07GF201J
R132	000432	RES	CARBON	4.3 K		5% 1/4W	81349	RC07GF432J
R133	000273	RES	CARBON	27 K		5% 1/4W	81349	RC07GF273J
R134	000201	RES	CARBON	200 OHM		5% 1/4W	81349	RC07GF201J
R135	000361	RES	CARBON	360 OHM		5% 1/4W	81349	RC07GF361J
R136	000101	RES	CARBON	100 OHM		5% 1/4W	81349	RC07GF101J
R137	010556	RES	METAL	3.48 K		1%	81349	RN60D3481F
R138	010556	RES	METAL	3.48 K		1%	81349	RN60D3481F
R139	010558	RES	CARBON	147 OHM		1%	81349	RN60D1470F
R140	000100	RES	CARBON	10 OHM		5% 1/4W	81349	RC07GF100J
R140	000333	RES	CARBON	33 K		5% 1/4W	81349	RC07GF333J
R141	010009	RES	METAL	1.62 K		1%	81349	RN60D1621F
R142	010557	RES	METAL	11.8 K		1%	81349	RN60D1182F
R143	000511	RES	CARBON	510 OHM		5% 1/4W	81349	RC07GF511J
R145	000431	RES	CARBON	430 OHM		5% 1/4W	81349	RC07GF431J
R146	000431	RES	CARBON	430 OHM		5% 1/4W	81349	RC07GF431J
R147	000751	RES	CARBON	750 OHM		5% 1/4W	81349	RC07GF751J
R148	000102	RES	CARBON	1 K		5% 1/4W	81349	RC07GF102J
R149	000202	RES	CARBON	2 K		5% 1/4W	81349	RC07GF202J

406047 – Assy., PCB, PROGRAM SIGNAL CONDITIONER – SINGLE *continued*

REF DES	DANA P/N	DESCRIPTION					FSC	MANU P/N
R150	000202	RES	CARBON	2 K		5% 1/4W	81349	RC07GF202J
R151	000431	RES	CARBON	430 OHM		5% 1/4W	81349	RC07GF431J
R152	000510	RES	CARBON	51 OHM		5% 1/4W	81349	RC07GF510J
R153	000103	RES	CARBON	10 K		5% 1/4W	81349	RC07GF103J
R154	000512	RES	CARBON	5.1 K		5% 1/4W	81349	RC07GF512J
R155	000512	RES	CARBON	5.1 K		5% 1/4W	81349	RC07GF512J
R156	000512	RES	CARBON	5.1 K		5% 1/4W	81349	RC07GF512J
R157	000512	RES	CARBON	5.1 K		5% 1/4W	81349	RC07GF512J
R158	000103	RES	CARBON	10 K		5% 1/4W	81349	RC07GF103J
R159	000103	RES	CARBON	10 K		5% 1/4W	81349	RC07GF103J
R160	000103	RES	CARBON	10 K		5% 1/4W	81349	RC07GF103J
R161	000512	RES	CARBON	5.1 K		5% 1/4W	81349	RC07GF512J
R162	000620	RES	CARBON	62 OHM		5% 1/4W	81349	RC07GF620J
R163	000302	RES	CARBON	3 K		5% 1/4W	81349	RC07GF302J
R164	000363	RES	CARBON	36 K		5% 1/4W	81349	RC07GF363J
R165	000512	RES	CARBON	5.1 K		5% 1/4W	81349	RC07GF512J
R166	000620	RES	CARBON	62 OHM		5% 1/4W	81349	RC07GF620J
R167	000302	RES	CARBON	3 K		5% 1/4W	81349	RC07GF302J
R168	000363	RES	CARBON	36 K		5% 1/4W	81349	RC07GF363J
R169	000620	RES	CARBON	62 OHM		5% 1/4W	81349	RC07GF620J
R170	000302	RES	CARBON	3 K		5% 1/4W	81349	RC07GF302J
R171	000363	RES	CARBON	36 K		5% 1/4W	81349	RC07GF363J
R172	000471	RES	CARBON	470 OHM		5% 1/4W	81349	RC07GF471J
R173	000681	RES	CARBON	680 OHM		5% 1/4W	81349	RC07GF681J
R174	000103	RES	CARBON	10 K		5% 1/4W	81349	RC07GF103J
R175	000820	RES	CARBON	82 OHM		5% 1/4W	81349	RC07GF820J
R176	000820	RES	CARBON	82 OHM		5% 1/4W	81349	RC07GF820J
R177	000472	RES	CARBON	4.7 K		5% 1/4W	81349	RC07GF472J
R178	000472	RES	CARBON	4.7 K		5% 1/4W	81349	RC07GF472J
R179	010082	RES	METAL	9.31 K	T-0	1%	81349	RN60D9311F
R180	010370	RES	METAL	9.76 K		1%	81349	RN60D9761F
R181	010125	RES	METAL	16.2 K		1% 1/4W	81349	RN60D1622F
R182	000302	RES	CARBON	3 K		5% 1/4W	81349	RC07GF302J
R183	000433	RES	CARBON	43 K		5% 1/4W	81349	RC07GF433J
R184	010234	RES	METAL	33.2 K	T-0	1%	81349	RN60D3322F
R185	040087	POT	CERMET	10 K		10%	73138	62PR10K
R186	010502	RES	METAL	249 K		1% 1/8W	81349	RN60D2493F
R187	010325	RES	METAL	43.2 K		1%	81349	RN60D4322F
R188	010503	RES	METAL	102 K		1% 1/8W	81349	RN60D1023F
R189	010325	RES	METAL	43.2 K		1%	81349	RN60D4322F
R190	010504	RES	METAL	29.4 K		1% 1/8W	81349	RN60D2942F
R191	010325	RES	METAL	43.2 K		1%	81349	RN60D4322F

406047 – Assy., PCB, PROGRAM SIGNAL CONDITIONER – SINGLE *continued*

REF DES	DANA P/N	DESCRIPTION					FSC	MANU P/N
R192	010209	RES	METAL	18.2 K	T-0	1%	81349	RN60D1822F
R193	010209	RES	METAL	18.2 K	T-0	1%	81349	RN60D1822F
R194	000134	RES	CARBON	130 K		5% 1/4W	81349	RC07GF134J
R195	000103	RES	CARBON	10 K		5% 1/4W	81349	RC07GF103J
R196	000512	RES	CARBON	5.1 K		5% 1/4W	81349	RC07GF512J
R197	000134	RES	CARBON	130 K		5% 1/4W	81349	RC07GF134J
R198	000103	RES	CARBON	10 K		5% 1/4W	81349	RC07GF103J
R199	000512	RES	CARBON	5.1 K		5% 1/4W	81349	RC07GF512J
R200	000134	RES	CARBON	130 K		5% 1/4W	81349	RC07GF134J
R201	000103	RES	CARBON	10 K		5% 1/4W	81349	RC07GF103J
R202	000512	RES	CARBON	5.1 K		5% 1/4W	81349	RC07GF512J
R203	000134	RES	CARBON	130 K		5% 1/4W	81349	RC07GF134J
R204	000103	RES	CARBON	10 K		5% 1/4W	81349	RC07GF103J
R205	000512	RES	CARBON	5.1 K		5% 1/4W	81349	RC07GF512J

406049 – Assy., PCB, PROGRAM SIGNAL CONDITIONER – DUAL

REF DES	DANA P/N	DESCRIPTION					FSC	MANU P/N
C1	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C2	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C3	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C4	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C5	110120	CAP	TANTA	4.7 MFD	25 V	10%	05397	T368B475K025AS
C6	110120	CAP	TANTA	4.7 MFD	25 V	10%	05397	T368B475K025AS
C7	110134	CAP	TANTA	33 MFD	10 V	20%	05397	T310B336M010AS
C101	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C102	100009	CAP	CERAM	5 PFD		10%	71471	TCDI-1 (N750)
C103	100057	CAP	CERAM	.1 MFD	500 V	20%	56289	5GA-P10
C104	100041	CAP	CERAM	25 PFD	1000 V	5%	56289	10TCCQ25
C105	130144	CAP	MICA	270 PFD	100 V	5%	72136	DM10271J
C106	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C107	130066	CAP	MICA	100 PFD	500 V	5%	09023	C015FD101J03
C108	130083	CAP	MICA	750 PFD	CM06FD751J03		72136	CM06FD751J03
C109	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C110	130076	CAP	MICA	200 PFD	500 V	5%	72136	DM15-201J
C111	130091	CAP	MICA	.0016 PFD	500 V	5%	72136	CM06F162J03
C112	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C113	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C114	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C115	101174	CAP	CERAM	.001 MFD	500 V	10%	71471	SCD3X5F
C116	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C117	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C118	100024	CAP		.1 MFD	5815-000Y5U104Z		72982	5815-000Y5U104Z
C119	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C120	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C121	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C122	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C123	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C124	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C125	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C126	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C127	110134	CAP	TANTA	33 MFD	10 V	20%	05397	T310B336M010AS
C301	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C302	100009	CAP	CERAM	5 PFD		10%	71471	TCDI-1 (N750)
C303	100057	CAP	CERAM	.1 MFD	500 V	20%	56289	5GA-P10
C304	100041	CAP	CERAM	25 PFD	1000 V	5%	56289	10TCCQ25
C305	130065	CAP	MICA	330 PFD	500 V	5%	09023	C015FD331J03
C306	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C307	130066	CAP	MICA	100 PFD	500 V	5%	09023	C015FD101J03

406049 – Assy., PCB, PROGRAM SIGNAL CONDITIONER – DUAL *continued*

REF DES	DANA P/N	DESCRIPTION					FSC	MANU P/N
C308	130083	CAP	MICA	750 PFD	CM06FD751J03		72136	CM06FD751J03
C309	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C310	130076	CAP	MICA	200 PFD	500 V	5%	72136	DM15-201J
C311	130091	CAP	MICA	.0016 PFD	500V	5%	72136	CM06F162J03
C312	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C313	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C314	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C315	101174	CAP	CERAM	.001 MFD	500 V	10%	71471	SCD3X5F
C316	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C317	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C318	100024	CAP	CERAM	.1 MFD	5815-000Y5U104Z		72982	5815-000Y5U104Z
C319	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C320	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C321	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C322	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C323	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C324	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C325	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C326	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C327	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	TG-S10
C328	110134	CAP	TANTA	33 MFD	10 V	20%	05397	T310B336M010AS
CR1	211083	DIODE	SILICO		018		21793	211083
CR101	211083	DIODE	SILICO		018		21793	211083
CR102	211083	DIODE	SILICO		018		21793	211083
CR103	211236	DIODE	SILICO		007		21793	211236
CR104	211236	DIODE	SILICO		007		21793	211236
CR105	211236	DIODE	SILICO		007		21793	211236
CR106	211236	DIODE	SILICO		007		21793	211236
CR107	210013	DIODE	SILICO		1N916		81349	1N916
CR108	210013	DIODE	SILICO		1N916		81349	1N916
CR109	210013	DIODE	SILICO		1N916		81349	1N916
CR110	210013	DIODE	SILICO		1N916		81349	1N916
CR111	210013	DIODE	SILICO		1N916		81349	1N916
CR112	210013	DIODE	SILICO		1N916		81349	1N916
CR113	211083	DIODE	SILICO		018		21793	211083
CR114	211083	DIODE	SILICO		018		21793	211083
CR115	211083	DIODE	SILICO		018		21793	211083
CR116	211083	DIODE	SILICO		018		21793	211083
CR117	211083	DIODE	SILICO		018		21793	211083
CR118	211083	DIODE	SILICO		018		21793	211083
CR119	211083	DIODE	SILICO		018		21793	211083

406049 – Assy., PCB, PROGRAM SIGNAL CONDITIONER – DUAL *continued*

REF DES	DANA P/N	DESCRIPTION	FSC	MANU P/N
CR120	211083	DIODE SILICO 018	21793	211083
CR121	211083	DIODE SILICO 018	21793	211083
CR122	211083	DIODE SILICO 018	21793	211083
CR123	211083	DIODE SILICO 018	21793	211083
CR124	211083	DIODE SILICO 018	21793	211083
CR125	211083	DIODE SILICO 018	21793	211083
CR126	211083	DIODE SILICO 018	21793	211083
CR127	211083	DIODE SILICO 018	21793	211083
CR128	211236	DIODE SILICO 007	21793	211236
CR129	211236	DIODE SILICO 007	21793	211236
CR130	220031	DIODE SILICO ZENER 1/4M3.3AZ5	04713	1/4M3.3AZ5
CR131	220031	DIODE SILICO ZENER 1/4M3.3AZ5	04713	1/4M3.3AZ5
CR301	211083	DIODE SILICO 018	21793	211083
CR302	211083	DIODE SILICO 018	21793	211083
CR303	211236	DIODE SILICO 007	21793	211236
CR304	211236	DIODE SILICO 007	21793	211236
CR305	211236	DIODE SILICO 007	21793	211236
CR306	211236	DIODE SILICO 007	21793	211236
CR307	210013	DIODE SILICO 1N916	81349	1N916
CR308	210013	DIODE SILICO 1N916	81349	1N916
CR309	210013	DIODE SILICO 1N916	81349	1N916
CR310	210013	DIODE SILICO 1N916	81349	1N916
CR311	210013	DIODE SILICO 1N916	81349	1N916
CR312	210013	DIODE SILICO 1N916	81349	1N916
CR313	211083	DIODE SILICO 018	21793	211083
CR314	211083	DIODE SILICO 018	21793	211083
CR315	211083	DIODE SILICO 018	21793	211083
CR316	211083	DIODE SILICO 018	21793	211083
CR317	211083	DIODE SILICO 018	21793	211083
CR318	211083	DIODE SILICO 018	21793	211083
CR319	211083	DIODE SILICO 018	21793	211083
CR320	211083	DIODE SILICO 018	21793	211083
CR321	211083	DIODE SILICO 018	21793	211083
CR322	211083	DIODE SILICO 018	21793	211083
CR323	211083	DIODE SILICO 018	21793	211083
CR324	211083	DIODE SILICO 018	21793	211083
CR325	211083	DIODE SILICO 018	21793	211083
CR326	211083	DIODE SILICO 018	21793	211083
CR327	211083	DIODE SILICO 018	21793	211083
CR328	211236	DIODE SILICO 007	21793	211236
CR329	211236	DIODE SILICO 007	21793	211236

406049 – Assy., PCB, PROGRAM SIGNAL CONDITIONER – DUAL *continued*

REF DES	DANA P/N	DESCRIPTION	FSC	MANU P/N
CR330	220031	DIODE SILICO ZENER 1/4M3.3AZ5	04713	1/4M3.3AZ5
CR331	220031	DIODE SILICO ZENER 1/4M3.3AZ5	04713	1/4M3.3AZ5
K1	310029	RELAY AZ420-56	26806	AZ420-56
L1	310062	CHOKE RF 22 µH 10%	99800	1537-44
L2	310062	CHOKE RF 22 µH 10%	99800	1537-44
L3	310062	CHOKE RF 22 µH 10%	99800	1537-44
L4	310062	CHOKE RF 22 µH 10%	99800	1537-44
L5	310070	CHOKE RF 5.6 µH 10%	99800	1537 Series
L101	310070	CHOKE RF 5.6 µH 10%	99800	1537 Series
L102	310068	CHOKE RF 1 µH 10%	99800	1537-12
L103	310070	CHOKE RF 5.6 µH 10%	99800	1537 Series
L301	310070	CHOKE RF 5.6 µH 10%	99800	1537 Series
L302	310068	CHOKE RF 1 µH 10%	99800	1537-12
L303	310070	CHOKE RF 5.6 µH 10%	99800	1537 Series
M1	230069	INTEGRATED CIRCUIT MC4007	04713	MC4007
M2	230028	INTEGRATED CIRCUIT SN7400N	01295	SN7400N
M3	230028	INTEGRATED CIRCUIT SN7400N	01295	SN7400N
M4	230028	INTEGRATED CIRCUIT SN7400N	01295	SN7400N
M5	230028	INTEGRATED CIRCUIT SN7400N	01295	SN7400N
M6	230028	INTEGRATED CIRCUIT SN7400N	01295	SN7400N
M7	230028	INTEGRATED CIRCUIT SN7400N	01295	SN7400N
M8	230040	INTEGRATED CIRCUIT MC1013P	04713	MC1013P
M9	230028	INTEGRATED CIRCUIT SN7400N	01295	SN7400N
M101	230028	INTEGRATED CIRCUIT SN7400N	01295	SN7400N
M102	230031	INTEGRATED CIRCUIT SN7410N	01295	SN7410N
M103	230043	INTEGRATED CIRCUIT MC1010P	04713	MC1010P
M104	230045	INTEGRATED CIRCUIT µA741C	07263	U6E7741393
M105	230028	INTEGRATED CIRCUIT SN7400N	01295	SN7400N
M301	230028	INTEGRATED CIRCUIT SN7400N	01295	SN7400N
M304	230045	INTEGRATED CIRCUIT µA741C	07263	U6E7741393
M305	230028	INTEGRATED CIRCUIT SN7400N	01295	SN7400N
Q1	200099	TRANS 2N4258	81349	2N4258
Q2	200088	TRANS SILICO PNP 2N4248	80131	2N4248
Q3	200037	TRANS SILICO NPN 2N3646	80131	2N3646
Q101	200068	TRANS 2N4250	80131	2N4250
Q102	200068	TRANS 2N4250	80131	2N4250
Q103	200173	TRANS MATCHED SET	21793	200173
Q104	200173	TRANS MATCHED SET	21793	200173

406049 – Assy., PCB, PROGRAM SIGNAL CONDITIONER – DUAL *continued*

REF DES	DANA P/N	DESCRIPTION	FSC	MANU P/N
Q105	200173	TRANS MATCHED SET	21793	200173
Q106	200173	TRANS MATCHED SET	21793	200173
Q107	200173	TRANS MATCHED SET	21793	200173
Q108	200068	TRANS 2N4250	80131	2N4250
Q109	200068	TRANS 2N4250	80131	2N4250
Q110	200068	TRANS 2N4250	80131	2N4250
Q111	200043	TRANS 200043	21793	200043
Q112	200173	TRANS MATCHED SET	21793	200173
Q113	200099	TRANS 2N4258	81349	2N4258
Q114	200151	TRANS SILICO 2N5179	81349	2N5179
Q115	200186	TRANS MATCHED SET	21793	200186
Q116	200151	TRANS SILICO 2N5179	81349	2N5179
Q117	200151	TRANS SILICO 2N5179	81349	2N5179
Q118	200186	TRANS MATCHED SET	21793	200186
Q119	200151	TRANS SILICO 2N5179	81349	2N5179
Q120	200082	TRANS 2N4424	81349	2N4424
Q121	200082	TRANS 2N4424	81349	2N4424
Q122	200082	TRANS 2N4424	81349	2N4424
Q123	200043	TRANS 200043	21793	200043
Q124	200043	TRANS 200043	21793	200043
Q125	200043	TRANS 200043	21793	200043
Q126	200043	TRANS 200043	21793	200043
Q127	200043	TRANS 200043	21793	200043
Q301	200068	TRANS 2N4250	80131	2N4250
Q302	200068	TRANS 2N4250	80131	2N4250
Q303	200173	TRANS MATCHED SET	21793	200173
Q304	200173	TRANS MATCHED SET	21793	200173
Q305	200173	TRANS MATCHED SET	21793	200173
Q306	200173	TRANS MATCHED SET	21793	200173
Q307	200173	TRANS MATCHED SET	21793	200173
Q308	200068	TRANS 2N4250	80131	2N4250
Q309	200068	TRANS 2N4250	80131	2N4250
Q310	200068	TRANS 2N4250	80131	2N4250
Q311	200043	TRANS 200043	21793	200043
Q312	200173	TRANS MATCHED SET	21793	200173
Q313	200099	TRANS 2N4258	81349	2N4258
Q314	200151	TRANS SILICO 2N5179	81349	2N5179
Q315	200186	TRANS MATCHED SET	21793	200186
Q316	200151	TRANS SILICO 2N5179	81349	2N5179
Q317	200151	TRANS SILICO 2N5179	81349	2N5179
Q318	200186	TRANS MATCHED SET	21793	200186
Q319	200151	TRANS SILICO 2N5179	81349	2N5179

406049 – Assy., PCB, PROGRAM SIGNAL CONDITIONER – DUAL *continued*

REF DES	DANA P/N	DESCRIPTION					FSC	MANU P/N
Q320	200082	TRANS			2N4424		81349	2N4424
Q321	200082	TRANS			2N4424		81349	2N4424
Q322	200082	TRANS			2N4424		81349	2N4424
Q323	200043	TRANS			200043		21793	200043
Q324	200043	TRANS			200043		21793	200043
Q325	200043	TRANS			200043		21793	200043
Q326	200043	TRANS			200043		21793	200043
Q327	200043	TRANS			200043		21793	200043
R1	000202	RES	CARBON	2 K		5% 1/4W	81349	RC07GF202J
R2	000202	RES	CARBON	2 K		5% 1/4W	81349	RC07GF202J
R3	000202	RES	CARBON	2 K		5% 1/4W	81349	RC07GF202J
R4	000202	RES	CARBON	2 K		5% 1/4W	81349	RC07GF202J
R5	000202	RES	CARBON	2 K		5% 1/4W	81349	RC07GF202J
R6	000202	RES	CARBON	2 K		5% 1/4W	81349	RC07GF202J
R7	000202	RES	CARBON	2 K		5% 1/4W	81349	RC07GF202J
R8	000101	RES	CARBON	100 OHM		5% 1/4W	81349	RC07GF101J
R9	000332	RES	CARBON	3.3 K		5% 1/4W	81349	RC07GF332J
R10	000392	RES	CARBON	3.9 K		5% 1/4W	81349	RC07GF392J
R11	000511	RES	CARBON	510 OHM		5% 1/4W	81349	RC07GF511J
R12	000202	RES	CARBON	2 K		5% 1/4W	81349	RC07GF202J
R13	000202	RES	CARBON	2 K		5% 1/4W	81349	RC07GF202J
R14	000270	RES	CARBON	27 OHM		5% 1/4W	81349	RC07GF270J
R15	000511	RES	CARBON	510 OHM		5% 1/4W	81349	RC07GF511J
R16	000101	RES	CARBON	100 OHM		5% 1/4W	81349	RC07GF101J
R17	000102	RES	CARBON	1 K		5% 1/4W	81349	RC07GF102J
R18	000153	RES	CARBON	15 K		5% 1/4W	81349	RC07GF153J
R101	000203	RES	CARBON	20 K		5% 1/4W	81349	RC07GF203J
R102	000151	RES	CARBON	150 OHM		5% 1/4W	81349	RC07GF151J
R103	000203	RES	CARBON	20 K		5% 1/4W	81349	RC07GF203J
R104	010496	RES	METAL	1 M	T-0	1% 1/8W	81349	RN60D
R105	010496	RES	METAL	1 M	T-0	1% 1/8W	81349	RN60D
R106	000202	RES	CARBON	2 K		5% 1/4W	81349	RC07GF202J
R107	000102	RES	CARBON	1 K		5% 1/4W	81349	RC07GF102J
R108	000102	RES	CARBON	1 K		5% 1/4W	81349	RC07GF102J
R109	000103	RES	CARBON	10 K		5% 1/4W	81349	RC07GF103J
R110	000153	RES	CARBON	15 K		5% 1/4W	81349	RC07GF153J
R111	000153	RES	CARBON	15 K		5% 1/4W	81349	RC07GF153J
R112	000153	RES	CARBON	15 K		5% 1/4W	81349	RC07GF153J
R113	000153	RES	CARBON	15 K		5% 1/4W	81349	RC07GF153J
R114	010376	RES	METAL	60.4 K	T-0	1%	81349	RN60D6042F

406049 – Assy., PCB, PROGRAM SIGNAL CONDITIONER – DUAL *continued*

REF DES	DANA P/N	DESCRIPTION					FSC	MANU P/N
R115	010513	RES	METAL	6.65 K		1% 1/4W	81349	RN60D6651F
R116	010287	RES	METAL	3.01 K	T-0	1%	81349	RN60D3011F
R117	010414	RES	METAL	825 OHM		1%	81349	RN60D8250F
R118	000135	RES	CARBON	1.3 M		5% 1/4W	81349	RC07GF135J
R119	000105	RES	CARBON	1 M		5% 1/4W	81349	RC07GF105J
R120	010124	RES	METAL	19.6 K	T-0	1% 1/4W	81349	RN60D1962F
R121	406524	RES	KIT, SELECTED		406524		21793	406524
R122	040098	POT	CERMET	20 OHM	62PR20		73138	62PR20
R123	011253	RES	METAL	4.75 K	T-0	1% 1/4W	81349	RN60D4751F
R124	000431	RES	CARBON	430 OHM		5% 1/4W	81349	RC07GF431J
R125	000100	RES	CARBON	10 OHM		5% 1/4W	81349	RC07GF100J
R126	000361	RES	CARBON	360 OHM		5% 1/4W	81349	RC07GF361J
R127	000101	RES	CARBON	100 OHM		5% 1/4W	81349	RC07GF101J
R128	000302	RES	CARBON	3 K		5% 1/4W	81349	RC07GF302J
R129	000201	RES	CARBON	200 OHM		5% 1/4W	81349	RC07GF201J
R130	000273	RES	CARBON	27 K		5% 1/4W	81349	RC07GF273J
R131	000201	RES	CARBON	200 OHM		5% 1/4W	81349	RC07GF201J
R132	000432	RES	CARBON	4.3 K		5% 1/4W	81349	RC07GF432J
R133	000273	RES	CARBON	27 K		5% 1/4W	81349	RC07GF273J
R134	000201	RES	CARBON	200 OHM		5% 1/4W	81349	RC07GF201J
R135	000361	RES	CARBON	360 OHM		5% 1/4W	81349	RC07GF361J
R136	000101	RES	CARBON	100 OHM		5% 1/4W	81349	RC07GF101J
R137	010556	RES	METAL	3.48 K		1%	81349	RN60D3481F
R138	010556	RES	METAL	3.48 K		1%	81349	RN60D3481F
R139	010558	RES	METAL	147 OHM		1%	81349	RN60D1470F
R140	000683	RES	CARBON	68 K		5% 1/4W	81349	RC07GF683J
R141	010009	RES	METAL	1.62 K		1% 1/4W	81349	RN60D1621F
R142	010278	RES	METAL	13.3 K	T-0	1%	81349	RN60D1332F
R143	000511	RES	CARBON	510 OHM		5% 1/4W	81349	RC07GF511J
R145	000431	RES	CARBON	430 OHM		5% 1/4W	81349	RC07GF431J
R146	000431	RES	CARBON	430 OHM		5% 1/4W	81349	RC07GF431J
R147	000751	RES	CARBON	750 OHM		5% 1/4W	81349	RC07GF751J
R148	000102	RES	CARBON	1 K		5% 1/4W	81349	RC07GF102J
R149	000202	RES	CARBON	2 K		5% 1/4W	81349	RC07GF202J
R150	000202	RES	CARBON	2 K		5% 1/4W	81349	RC07GF202J
R151	000431	RES	CARBON	430 OHM		5% 1/4W	81349	RC07GF431J
R152	000510	RES	CARBON	51 OHM		5% 1/4W	81349	RC07GF510J
R153	000103	RES	CARBON	10 K		5% 1/4W	81349	RC07GF103J
R154	000512	RES	CARBON	5.1 K		5% 1/4W	81349	RC07GF512J
R155	000512	RES	CARBON	5.1 K		5% 1/4W	81349	RC07GF512J
R156	000512	RES	CARBON	5.1 K		5% 1/4W	81349	RC07GF512J
R157	000512	RES	CARBON	5.1 K		5% 1/4W	81349	RC07GF512J

406049 – Assy., PCB, PROGRAM SIGNAL CONDITIONER – DUAL *continued*

REF DES	DANA P/N	DESCRIPTION					FSC	MANU P/N
R158	000103	RES	CARBON	10 K		5% 1/4W	81349	RC07GF103J
R159	000103	RES	CARBON	10 K		5% 1/4W	81349	RC07GF103J
R160	000103	RES	CARBON	10 K		5% 1/4W	81349	RC07GF103J
R161	000512	RES	CARBON	5.1 K		5% 1/4W	81349	RC07GF512J
R162	000620	RES	CARBON	62 OHM		5% 1/4W	81349	RC07GF620J
R163	000302	RES	CARBON	3 K		5% 1/4W	81349	RC07GF302J
R164	000363	RES	CARBON	36 K		5% 1/4W	81349	RC07GF363J
R165	000512	RES	CARBON	5.1 K		5% 1/4W	81349	RC07GF512J
R166	000620	RES	CARBON	62 OHM		5% 1/4W	81349	RC07GF620J
R167	000302	RES	CARBON	3 K		5% 1/4W	81349	RC07GF302J
R168	000363	RES	CARBON	36 K		5% 1/4W	81349	RC07GF363J
R169	000620	RES	CARBON	62 OHM		5% 1/4W	81349	RC07GF620J
R170	000302	RES	CARBON	3 K		5% 1/4W	81349	RC07GF302J
R171	000363	RES	CARBON	36 K		5% 1/4W	81349	RC07GF363J
R172	000471	RES	CARBON	470 OHM		5% 1/4W	81349	RC07GF471J
R173	000681	RES	CARBON	680 OHM		5% 1/4W	81349	RC07GF681J
R174	000103	RES	CARBON	10 K		5% 1/4W	81349	RC07GF103J
R175	000820	RES	CARBON	82 OHM		5% 1/4W	81349	RC07GF820J
R176	000820	RES	CARBON	82 OHM		5% 1/4W	81349	RC07GF820J
R177	000472	RES	CARBON	4.7 K		5% 1/4W	81349	RC07GF472J
R178	000472	RES	CARBON	4.7 K		5% 1/4W	81349	RC07GF472J
R179	010082	RES	METAL	9.31 K	T-0	1%	81349	RN60D9311F
R180	010370	RES	METAL	9.76 K		1%	81349	RN60D9761F
R181	010814	RES	METAL	15.8 K		1%	81349	RN55C
R182	000302	RES	CARBON	3 K		5% 1/4W	81349	RC07GF302J
R183	000433	RES	CARBON	43 K		5% 1/4W	81349	RC07GF433J
R184	010817	RES	METAL	33.2 K		1%	81349	RN55C
R185	040087	POT	CERMET	10 K		10%	73138	62PR10K
R186	010819	RES	METAL	249 K		1%	81349	RN55C
R187	010818	RES	METAL	43.2 K		1%	81349	RN55C
R188	010820	RES	METAL	102 K		1%	81349	RN55C
R189	010818	RES	METAL	43.2 K		1%	81349	RN55C
R190	010816	RES	METAL	29.4 K		1%	81349	RN55C
R191	010818	RES	METAL	43.2 K		1%	81349	RN55C
R192	010815	RES	METAL	18.2 K		1%	81349	RN55C
R193	010815	RES	METAL	18.2 K		1%	81349	RN55C
R194	000134	RES	CARBON	130 K		5% 1/4W	81349	RC07GF134J
R195	000103	RES	CARBON	10 K		5% 1/4W	81349	RC07GF103J
R196	000512	RES	CARBON	5.1 K		5% 1/4W	81349	RC07GF512J
R197	000134	RES	CARBON	130 K		5% 1/4W	81349	RC07GF134J
R198	000103	RES	CARBON	10 K		5% 1/4W	81349	RC07GF103J
R199	000512	RES	CARBON	5.1 K		5% 1/4W	81349	RC07GF512J

406049 – Assy., PCB, PROGRAM SIGNAL CONDITIONER – DUAL *continued*

REF DES	DANA P/N	DESCRIPTION					FSC	MANU P/N
R200	000134	RES	CARBON	130 K		5% 1/4W	81349	RC07GF134J
R201	000103	RES	CARBON	10 K		5% 1/4W	81349	RC07GF103J
R202	000512	RES	CARBON	5.1 K		5% 1/4W	81349	RC07GF512J
R203	000134	RES	CARBON	130 K		5% 1/4W	81349	RC07GF134J
R204	000103	RES	CARBON	10 K		5% 1/4W	81349	RC07GF103J
R205	000512	RES	CARBON	5.1 K		5% 1/4W	81349	RC07GF512J
R206	010719	RES	METAL	16.2 K		1%	81349	RN55D1622F
R207	010719	RES	METAL	16.2 K		1%	81349	RN55D1622F
R301	000203	RES	CARBON	20 K		5% 1/4W	81349	RC07GF203J
R302	000151	RES	CARBON	150 OHM		5% 1/4W	81349	RC07GF151J
R303	000203	RES	CARBON	20 K		5% 1/4W	81349	RC07GF203J
R304	010496	RES	METAL	1 M	T-0	1% 1/8W	81349	RN60D
R305	010496	RES	METAL	1 M	T-0	1% 1/8W	81349	RN60D
R306	000202	RES	CARBON	2 K		5% 1/4W	81349	RC07GF202J
R307	000102	RES	CARBON	1 K		5% 1/4W	81349	RC07GF102J
R308	000102	RES	CARBON	1 K		5% 1/4W	81349	RC07GF102J
R309	000103	RES	CARBON	10 K		5% 1/4W	81349	RC07GF103J
R310	000153	RES	CARBON	15 K		5% 1/4W	81349	RC07GF153J
R311	000153	RES	CARBON	15 K		5% 1/4W	81349	RC07GF153J
R312	000153	RES	CARBON	15 K		5% 1/4W	81349	RC07GF153J
R313	000153	RES	CARBON	15 K		5% 1/4W	81349	RC07GF153J
R314	010376	RES	METAL	60.4 K	T-0	1%	81349	RN60D6042F
R315	010513	RES	METAL	6.65 K		1% 1/4W	81349	RN60D6651F
R316	010287	RES	METAL	3.01 K	T-0	1%	81349	RN60D3011F
R317	010414	RES	METAL	825 OHM		1%	81349	RN60D8250F
R318	000135	RES	CARBON	1.3 M		5% 1/4W	81349	RC07GF135J
R319	000105	RES	CARBON	1 M		5% 1/4W	81349	RC07GF105J
R320	010124	RES	METAL	19.6 K	T-0	1% 1/4W	81349	RN60D1962F
R321	406524	RES	KIT, SELECTED		406524		21793	406524
R322	040098	POT	CERMET	20 OHM	62PR20		73138	62PR20
R323	011253	RES	METAL	4.75 K	T-0	1% 1/4W	81349	RN60D4751F
R324	000431	RES	CARBON	430 OHM		5% 1/4W	81349	RC07GF431J
R325	000100	RES	CARBON	10 OHM		5% 1/4W	81349	RC07GF100J
R326	000361	RES	CARBON	360 OHM		5% 1/4W	81349	RC07GF361J
R327	000101	RES	CARBON	100 OHM		5% 1/4W	81349	RC07GF101J
R328	000302	RES	CARBON	3 K		5% 1/4W	81349	RC07GF302J
R329	000201	RES	CARBON	200 OHM		5% 1/4W	81349	RC07GF201J
R330	000273	RES	CARBON	27 K		5% 1/4W	81349	RC07GF273J
R331	000201	RES	CARBON	200 OHM		5% 1/4W	81349	RC07GF201J
R332	000432	RES	CARBON	4.3 K		5% 1/4W	81349	RC07GF432J
R333	000273	RES	CARBON	27 K		5% 1/4W	81349	RC07GF273J
R334	000201	RES	CARBON	200 OHM		5% 1/4W	81349	RC07GF201J

406049 – Assy., PCB, PROGRAM SIGNAL CONDITIONER – DUAL *continued*

REF DES	DANA P/N	DESCRIPTION					FSC	MANU P/N
R335	000361	RES	CARBON	360 OHM		5% 1/4W	81349	RC07GF361J
R336	000101	RES	CARBON	100 OHM		5% 1/4W	81349	RC07GF101J
R337	010556	RES	METAL	3.48 K		1%	81349	RN60D3481F
R338	010556	RES	METAL	3.48 K		1%	81349	RN60D3481F
R339	010558	RES	METAL	147 OHM		1%	81349	RN60D1470F
R340	000513	RES	CARBON	51 K		5% 1/4W	81349	RC07GF513J
R341	010009	RES	METAL	1.62 K		1%	81349	RN60D1621F
R342	010278	RES	METAL	13.3 K	T-0	1%	81349	RN60D1332F
R343	000511	RES	CARBON	510 OHM		5% 1/4W	81349	RC07GF511J
R345	000431	RES	CARBON	430 OHM		5% 1/4W	81349	RC07GF431J
R346	000431	RES	CARBON	430 OHM		5% 1/4W	81349	RC07GF431J
R347	000751	RES	CARBON	750 OHM		5% 1/4W	81349	RC07GF751J
R348	000102	RES	CARBON	1 K		5% 1/4W	81349	RC07GF102J
R349	000202	RES	CARBON	2 K		5% 1/4W	81349	RC07GF202J
R350	000202	RES	CARBON	2 K		5% 1/4W	81349	RC07GF202J
R351	000431	RES	CARBON	430 OHM		5% 1/4W	81349	RC07GF431J
R353	000103	RES	CARBON	10 K		5% 1/4W	81349	RC07GF103J
R354	000512	RES	CARBON	5.1 K		5% 1/4W	81349	RC07GF512J
R355	000512	RES	CARBON	5.1 K		5% 1/4W	81349	RC07GF512J
R356	000512	RES	CARBON	5.1 K		5% 1/4W	81349	RC07GF512J
R357	000512	RES	CARBON	5.1 K		5% 1/4W	81349	RC07GF512J
R358	000103	RES	CARBON	10 K		5% 1/4W	81349	RC07GF103J
R359	000103	RES	CARBON	10 K		5% 1/4W	81349	RC07GF103J
R360	000103	RES	CARBON	10 K		5% 1/4W	81349	RC07GF103J
R361	000512	RES	CARBON	5.1 K		5% 1/4W	81349	RC07GF512J
R362	000620	RES	CARBON	62 OHM		5% 1/4W	81349	RC07GF620J
R363	000302	RES	CARBON	3 K		5% 1/4W	81349	RC07GF302J
R364	000363	RES	CARBON	36 K		5% 1/4W	81349	RC07GF363J
R365	000512	RES	CARBON	5.1 K		5% 1/4W	81349	RC07GF512J
R366	000620	RES	CARBON	62 OHM		5% 1/4W	81349	RC07GF620J
R367	000302	RES	CARBON	3 K		5% 1/4W	81349	RC07GF302J
R368	000363	RES	CARBON	36 K		5% 1/4W	81349	RC07GF363J
R369	000620	RES	CARBON	62 OHM		5% 1/4W	81349	RC07GF620J
R370	000302	RES	CARBON	3 K		5% 1/4W	81349	RC07GF302J
R371	000363	RES	CARBON	36 K		5% 1/4W	81349	RC07GF363J
R372	000471	RES	CARBON	470 OHM		5% 1/4W	81349	RC07GF471J
R373	000681	RES	CARBON	680 OHM		5% 1/4W	81349	RC07GF681J
R374	000103	RES	CARBON	10 K		5% 1/4W	81349	RC07GF103J
R375	000820	RES	CARBON	82 OHM		5% 1/4W	81349	RC07GF820J
R376	000820	RES	CARBON	82 OHM		5% 1/4W	81349	RC07GF820J
R377	000472	RES	CARBON	4.7 K		5% 1/4W	81349	RC07GF472J
R378	000472	RES	CARBON	4.7 K		5% 1/4W	81349	RC07GF472J

406049 – Assy., PCB, PROGRAM SIGNAL CONDITIONER – DUAL *continued*

REF DES	DANA P/N	DESCRIPTION					FSC	MANU P/N
R379	010082	RES	METAL	9.31 K	T-0	1%	81349	RN60D9311F
R380	010370	RES	METAL	9.76 K		1%	81349	RN60D9761F
R381	010814	RES	METAL	15.8 K		1%	81349	RN55C
R382	000302	RES	CARBON	3 K		5% 1/4W	81349	RC07GF302J
R383	000433	RES	CARBON	43 K		5% 1/4W	81349	RC07GF433J
R384	010817	RES	METAL	33.2 K		1%	81349	RN55C
R385	040087	POT	CERMET	10 K		10%	73138	62PR10K
R386	010819	RES	METAL	249 K		1%	81349	RN55C
R387	010818	RES	METAL	43.2 K		1%	81349	RN55C
R388	010820	RES	METAL	102 K		1%	81349	RN55C
R389	010818	RES	METAL	43.2 K		1%	81349	RN55C
R390	010816	RES	METAL	29.4 K		1%	81349	RN55C
R391	010818	RES	METAL	43.2 K		1%	81349	RN55C
R392	010815	RES	METAL	18.2 K		1%	81349	RN55C
R393	010815	RES	METAL	18.2 K		1%	81349	RN55C
R394	000134	RES	CARBON	130 K		5% 1/4W	81349	RC07GF134J
R395	000103	RES	CARBON	10 K		5% 1/4W	81349	RC07GF103J
R396	000512	RES	CARBON	5.1 K		5% 1/4W	81349	RC07GF512J
R397	000134	RES	CARBON	130 K		5% 1/4W	81349	RC07GF134J
R398	000103	RES	CARBON	10 K		5% 1/4W	81349	RC07GF103J
R399	000512	RES	CARBON	5.1 K		5% 1/4W	81349	RC07GF512J
R400	000134	RES	CARBON	130 K		5% 1/4W	81349	RC07GF134J
R401	000103	RES	CARBON	10 K		5% 1/4W	81349	RC07GF103J
R402	000512	RES	CARBON	5.1 K		5% 1/4W	81349	RC07GF512J
R403	000134	RES	CARBON	130 K		5% 1/4W	81349	RC07GF134J
R404	000103	RES	CARBON	10 K		5% 1/4W	81349	RC07GF103J
R405	000512	RES	CARBON	5.1 K		5% 1/4W	81349	RC07GF512J
R406	010719	RES	METAL	16.2 K		1%	81349	RN55D1622F
R407	010719	RES	METAL	16.2 K		1%	81349	RN55D1622F

406050 – Assy., PCB, ELECTRICAL OUTPUT

REF DES	DANA P/N	DESCRIPTION	FSC	MANU P/N
A1	230028	INTEGRATED CIRCUIT SN7400N	01295	SN7400N
A2	230028	INTEGRATED CIRCUIT SN7400N	01295	SN7400N
B1	230028	INTEGRATED CIRCUIT SN7400N	01295	SN7400N
B2	230028	INTEGRATED CIRCUIT SN7400N	01295	SN7400N
C1	230028	INTEGRATED CIRCUIT SN7400N	01295	SN7400N
C2	230028	INTEGRATED CIRCUIT SN7400N	01295	SN7400N
D1	230028	INTEGRATED CIRCUIT SN7400N	01295	SN7400N
D2	230028	INTEGRATED CIRCUIT SN7400N	01295	SN7400N
E1	230028	INTEGRATED CIRCUIT SN7400N	01295	SN7400N
E2	230028	INTEGRATED CIRCUIT SN7400N	01295	SN7400N
F1	230028	INTEGRATED CIRCUIT SN7400N	01295	SN7400N
F2	230028	INTEGRATED CIRCUIT SN7400N	01295	SN7400N
F3	230032	INTEGRATED CIRCUIT SN7420N	01295	SN7420N
F4	230031	INTEGRATED CIRCUIT SN7410N	01295	SN7410N
F5	230031	INTEGRATED CIRCUIT SN7410N	01295	SN7410N
F6	230028	INTEGRATED CIRCUIT SN7400N	01295	SN7400N
R1	000390	RES CARBON 39 OHM 5% 1/4W	81349	RC07GF390J
R2	000390	RES CARBON 39 OHM 5% 1/4W	81349	RC07GF390J
R3	000390	RES CARBON 39 OHM 5% 1/4W	81349	RC07GF390J
R4	000390	RES CARBON 39 OHM 5% 1/4W	81349	RC07GF390J
R5	000390	RES CARBON 39 OHM 5% 1/4W	81349	RC07GF390J
R6	000390	RES CARBON 39 OHM 5% 1/4W	81349	RC07GF390J
R7	000390	RES CARBON 39 OHM 5% 1/4W	81349	RC07GF390J
R8	000390	RES CARBON 39 OHM 5% 1/4W	81349	RC07GF390J
R9	000390	RES CARBON 39 OHM 5% 1/4W	81349	RC07GF390J
R10	000390	RES CARBON 39 OHM 5% 1/4W	81349	RC07GF390J
R11	000390	RES CARBON 39 OHM 5% 1/4W	81349	RC07GF390J
R12	000390	RES CARBON 39 OHM 5% 1/4W	81349	RC07GF390J
R13	000390	RES CARBON 39 OHM 5% 1/4W	81349	RC07GF390J
R14	000390	RES CARBON 39 OHM 5% 1/4W	81349	RC07GF390J
R15	000390	RES CARBON 39 OHM 5% 1/4W	81349	RC07GF390J
R16	000390	RES CARBON 39 OHM 5% 1/4W	81349	RC07GF390J
R17	000390	RES CARBON 39 OHM 5% 1/4W	81349	RC07GF390J
R18	000390	RES CARBON 39 OHM 5% 1/4W	81349	RC07GF390J
R19	000390	RES CARBON 39 OHM 5% 1/4W	81349	RC07GF390J
R20	000390	RES CARBON 39 OHM 5% 1/4W	81349	RC07GF390J
R21	000390	RES CARBON 39 OHM 5% 1/4W	81349	RC07GF390J
R22	000390	RES CARBON 39 OHM 5% 1/4W	81349	RC07GF390J
R23	000390	RES CARBON 39 OHM 5% 1/4W	81349	RC07GF390J
R24	000390	RES CARBON 39 OHM 5% 1/4W	81349	RC07GF390J
R25	000390	RES CARBON 39 OHM 5% 1/4W	81349	RC07GF390J

406050 – Assy., PCB, ELECTRICAL OUTPUT *continued*

REF DES	DANA P/N	DESCRIPTION				FSC	MANU P/N
R26	000390	RES	CARBON	39 OHM	5% 1/4W	81349	RC07GF390J
R27	000390	RES	CARBON	39 OHM	5% 1/4W	81349	RC07GF390J
R28	000390	RES	CARBON	39 OHM	5% 1/4W	81349	RC07GF390J
R29	000390	RES	CARBON	39 OHM	5% 1/4W	81349	RC07GF390J
R30	000390	RES	CARBON	39 OHM	5% 1/4W	81349	RC07GF390J
R31	000390	RES	CARBON	39 OHM	5% 1/4W	81349	RC07GF390J
R32	000390	RES	CARBON	39 OHM	5% 1/4W	81349	RC07GF390J
R33	000390	RES	CARBON	39 OHM	5% 1/4W	81349	RC07GF390J
R34	000390	RES	CARBON	39 OHM	5% 1/4W	81349	RC07GF390J
R35	000390	RES	CARBON	39 OHM	5% 1/4W	81349	RC07GF390J
R36	000390	RES	CARBON	39 OHM	5% 1/4W	81349	RC07GF390J
R37	000390	RES	CARBON	39 OHM	5% 1/4W	81349	RC07GF390J
R38	000390	RES	CARBON	39 OHM	5% 1/4W	81349	RC07GF390J
R39	000390	RES	CARBON	39 OHM	5% 1/4W	81349	RC07GF390J
R40	000390	RES	CARBON	39 OHM	5% 1/4W	81349	RC07GF390J
R41	000390	RES	CARBON	39 OHM	5% 1/4W	81349	RC07GF390J
R42	000390	RES	CARBON	39 OHM	5% 1/4W	81349	RC07GF390J
R43	000390	RES	CARBON	39 OHM	5% 1/4W	81349	RC07GF390J
R44	000390	RES	CARBON	39 OHM	5% 1/4W	81349	RC07GF390J
R45	000202	RES	CARBON	2 K	5% 1/4W	81349	RC07GF202J
R46	000202	RES	CARBON	2 K	5% 1/4W	81349	RC07GF202J
R47	000511	RES	CARBON	510 OHM	5% 1/4W	81349	RC07GF511J

SECTION 10

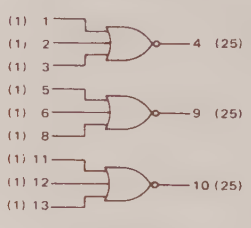
INTEGRATED CIRCUITS

10.1 INTEGRATED CIRCUITS

	Dana Part No.	Page
MECL 11 MC 1000/1200 Series		10-2
MC 1007P Triple Nor Gate	230041	10-2
MC 1010P Quad 2 Nor Gate	230043	10-2
MC 1013P 85 MHz J-K Flip-Flop	230040	10-2
MC 1022P Type D Flip-Flop	230068	10-2
MC 1461R Power Supply Voltage Regulator	350013	10-3
*MC 1670S Type D Flip-Flop	350012	10-4
SN 7400 Quadruple 2-Input Positive Nand Gates	230028	10-5
SN 7402 Quadruple 2-Input Positive Nor Gates	230030	10-5
SN 7410 Triple 3-Input Positive Nand Gates	230031	10-6
SN 7420 Dual 4-Input Positive Nand Gates	230032	10-6
SN 7430 8-Input Positive Nand Gates	230033	10-7
SN 7441A BCD-To-Decimal Decoder/Driver	230034	10-7
SN 7442 4-Line-To-10-Line Decoders (1-of-10)	350015	10-8
SN 7445 BCD-To-Decimal Decoders/Drivers	230033	10-9
SN 7474 Dual D-Type Edge-Triggered Flip-Flops	350005	10-9
SN 7475 8-Bit and 4-Bit Bistable Latches	350006	10-10
SN 7483 4-Bit Binary Full Adders	230036	10-11
SN 7490 Decade Counters	230027	10-12
SN 7491A 8-Bit Shift Registers	350007	10-13
SN 7496 5-Bit Shift Registers	350018	10-14
*μA 741C Operational Amplifier	350175	10-15

*8120 and 8130 only

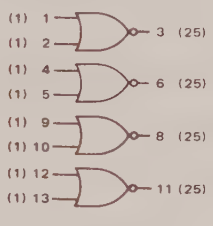
MC1007, MC1008, MC1009
MC1207, MC1208, MC1209
Triple 3-Input Gate



$4 = \overline{1 + 2 + 3}$

t_{pd} = 4.0 ns
P_D = MC1007/MC1207 – 110 mW
MC1008/MC1208 – 75 mW
MC1009/MC1209 – 60 mW

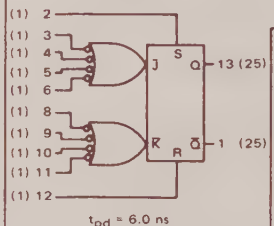
MC1010, MC1011, MC1012
MC1210, MC1211, MC1212
Quad 2-Input Gate



$3 = \overline{1 + 2}$

t_{pd} = 4.5 ns
P_D = MC1010/MC1210 – 115 mW
MC1011/MC1211 – 95 mW
MC1012/MC1212 – 65 mW

MC1013, MC1213
85 MHz AC-Coupled $\overline{J}$-$\overline{K}$ Flip Flop



t_{pd} = 6.0 ns
P_D = 125 mW

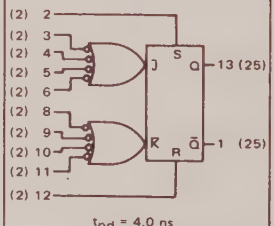
CLOCKED J-K OPERATION

J	$\overline{K}$	$\overline{C}_D$	Q^n
ϕ	ϕ	0	Q^n
0	0	1	$\overline{Q}^n$
0	1	1	1
1	0	1	0
1	1	1	Q^n

The J and $\overline{K}$ inputs refer to logic levels while the $\overline{C}_D$ input refers to dynamic logic swings. The J and $\overline{K}$ inputs should be changed to a logical "1" only while the $\overline{C}_D$ input is in a logic "1" state. ($\overline{C}_D$ maximum "1" level = V_{CC} – 0.6 V.) Clock $\overline{C}_D$ is obtained by tying one J and one $\overline{K}$ input together.

R-S OPERATION

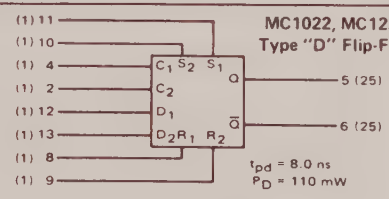
R	S	Q^{n+1}
0	1	1
1	0	0
0	0	Q^n
1	1	N.D.



t_{pd} = 4.0 ns
P_D = 250 mW

MC1027
120 MHz AC-Coupled $\overline{J}$-$\overline{K}$ Flip-Flop

MC1022, MC1222
Type "D" Flip-Flop



t_{pd} = 8.0 ns
P_D = 110 mW

R-S TRUTH TABLE

Pin No	R	S	Q^{n+1}	$\overline{Q}^{n+1}$
	8 or 9	10 or 11	5	6
	0	0	Q^n	$\overline{Q}^n$
	0	1	1	0
	1	0	0	1
	1	1	N.D.	N.D.

N.D. = Not Defined

CLOCKED TRUTH TABLE

Pin No	D	C	Q^{n+1}	$\overline{Q}^{n+1}$
	12 or 13	2 or 4	5	6
	0	0	Q^n	$\overline{Q}^n$
	1	0	Q^n	$\overline{Q}^n$
	0	1*	0	1
	1	1*	1	0

*A "1" on Clock input is defined for this flip-flop as a change in level from a low input to a high input

. . . designed to deliver load current up to 500 mA without use of an external power transistor

Typical Features:

- Electronic "Shut-Down" Control and Short-Circuit Protection
- Excellent Load Regulation (Low Output Impedance = 20 milliohms typ from dc to 100 kHz)
- High Power Capability: 17.5 W max @ 25°C (R Package)
- Excellent Transient Response and Temperature Stability
- High Ripple Rejection = 0.002 %/V typ
- Single External Transistor Can Boost Load Current to Greater Than 10 Amperes

Pin 10 electrically connected to case.

G SUFFIX
CASE 602A
(Formerly Case 71A)

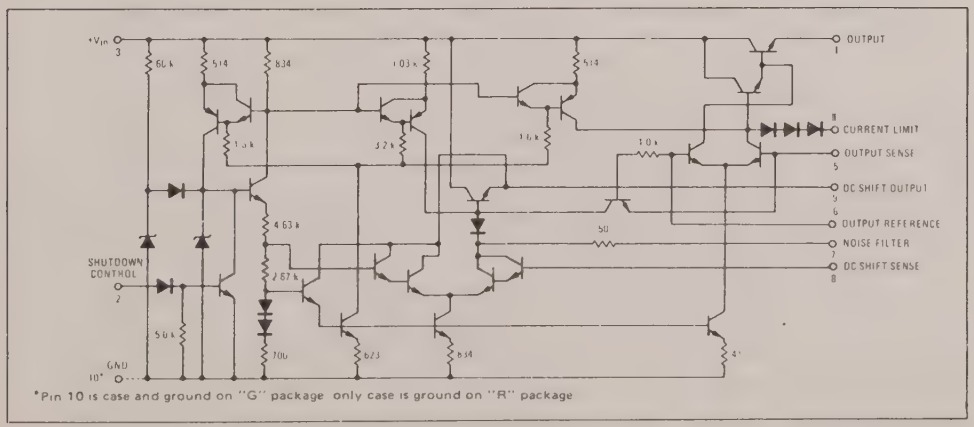
Case is ground terminal.

R SUFFIX
CASE 614

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

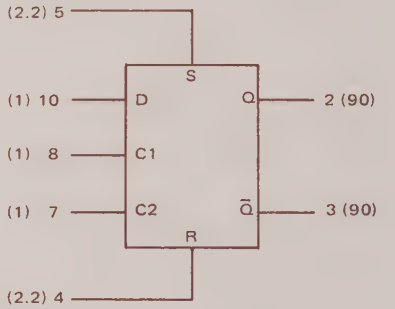
Rating	Symbol	Value		Unit
Input Voltage	V_{in}	35		Vdc
		G Package	R Package	
Load Current	I_L	200	500	mA
Current, Pin 2	$I_{pin\ 2}$	10	10	mA
Power Dissipation (Derate to T_J = 150°C) T_A = 25°C	P_D	0.68	2.0	Watts
Derate above T_A = 25°C		5.4	16	mW/°C
T_C = 25°C		1.8	17.5	Watts
Derate above T_C = 25°C		14.4	120	mW/°C
Operating Temperature Range MC1461 / MC1561	T_C	0 to +75 / -55 to +125		°C
Storage Temperature Range	T_{stg}	-65 to +150		C

CIRCUIT SCHEMATIC



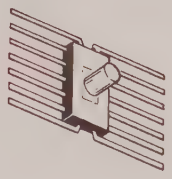
*Pin 10 is case and ground on "G" package only case is ground on "R" package

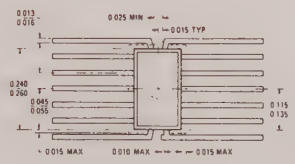
MC1670S
SINGLE PHASE TYPE D FLIP-FLOP

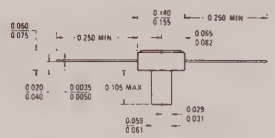


f_{Tog} = 350 MHz typ
P_D = 190 mW typ/pkg (no load)

MECL III STUD PACKAGE



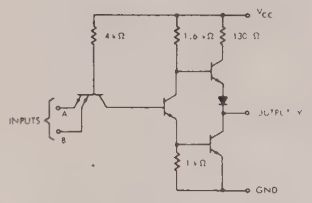




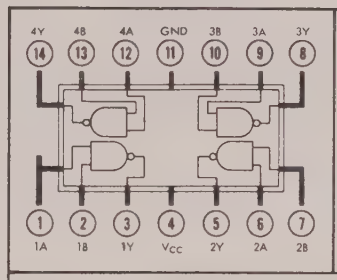
NOTE Lead No. 1 is identified by a tab on that lead

CASE 617
OUTLINE DIMENSIONS

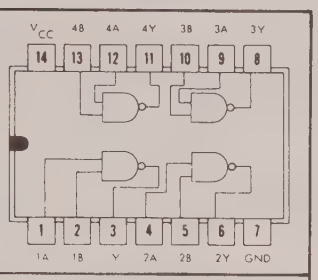
schematic (each gate)



F FLAT PACKAGE
(TOP VIEW)

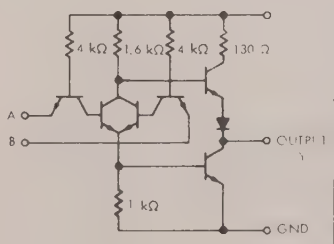


J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)

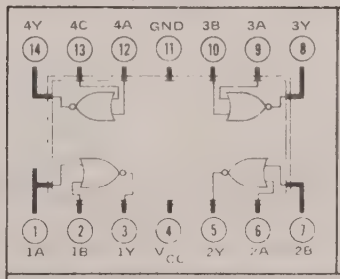


positive logic: $Y = \overline{AB}$

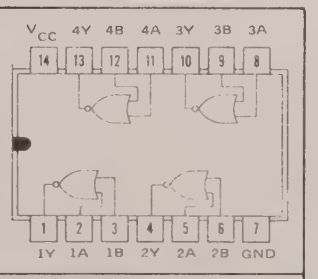
schematic (each gate)



S FLAT PACKAGE
(TOP VIEW)

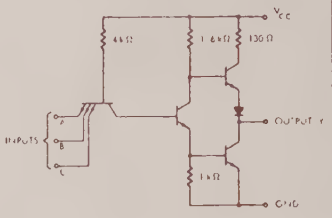


J OR N-DUAL-IN-LINE PACKAGE
(TOP VIEW)

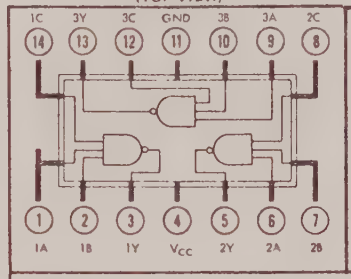


positive logic: $Y = \overline{A + B} = \overline{A} \cdot \overline{B}$

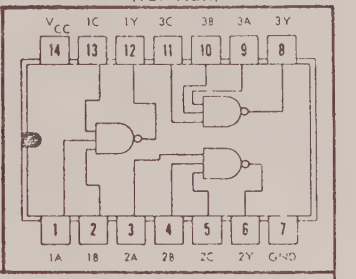
schematic (each gate)



S FLAT PACKAGE
(TOP VIEW)

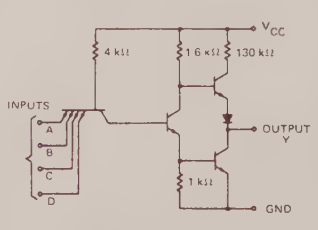


J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



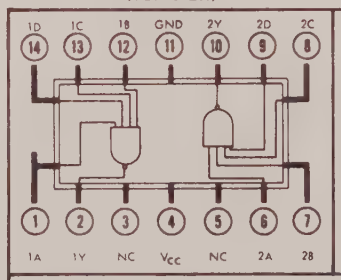
positive logic: $Y = \overline{ABC}$

schematic (each gate)

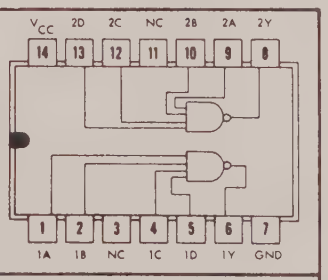


Component values shown are nominal.
NC—No Internal Connection

S FLAT PACKAGE
(TOP VIEW)

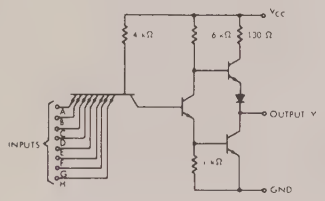


J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)

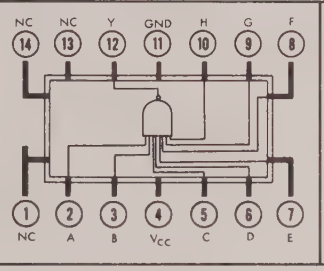


positive logic: $Y = \overline{ABCD}$

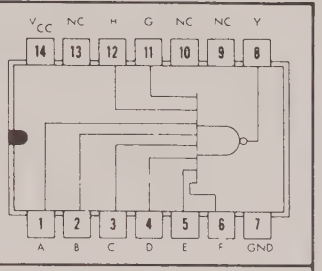
schematic



S FLAT PACKAGE
(TOP VIEW)



J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



positive logic: $Y = \overline{ABCDEFGH}$

SN7441A
BCD-TO-DECIMAL DECODER/DRIVER

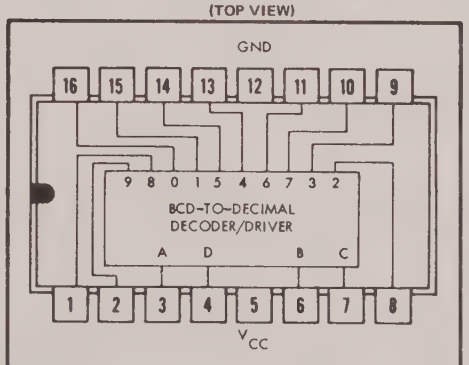
logic

TRUTH TABLE

INPUT				OUTPUT ON ‡
D	C	B	A	
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9

‡ All other outputs are off.

J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



positive logic: see truth table

description

The SN7441A is a monolithic, BCD-to-decimal decoder incorporating high performance output transistors designed for driving gas-filled, cold-cathode indicator tubes. The BCD-to-decimal decoder consists of familiar transistor-transistor-logic (TTL) gate circuits which select one of the ten decimal output drivers. The BCD inputs are fully compatible with Series 74 logic outputs; and, in addition, physical placement of these inputs is coincidental with the BCD output of the SN7490 decade counter. The ten high-breakdown, n-p-n transistors have a maximum reverse current of 50 μA at 55 V over the operating temperature range.

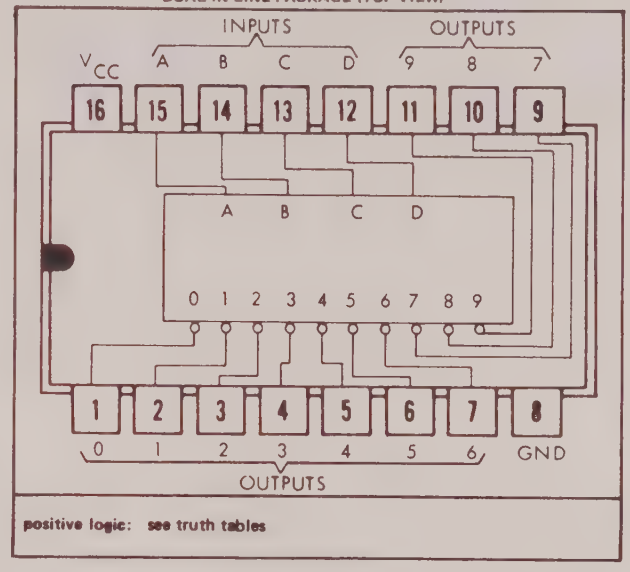
A typical application shows the SN7441A used as a gas-filled, display-indicator driver.

description

These monolithic decimal decoders consist of eight inverters and ten four-input NAND gates. The inverters are connected in pairs to make BCD input data available for decoding by the NAND gates. Full decoding of valid input logic ensures that all outputs remain off for all invalid input conditions.

The SN5442/SN7442 BCD-to-decimal, SN5443/SN7443 excess 3-to-decimal, and SN5444/SN7444 excess 3 gray-to-decimal decoders feature familiar transistor-transistor logic (TTL) circuits with inputs and outputs which are compatible for use with other TTL and DTL circuits. D-c noise margins are typically one volt and power dissipation is typically 140 milliwatts. Full fan-out of 10 is available at all outputs.

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: see truth tables

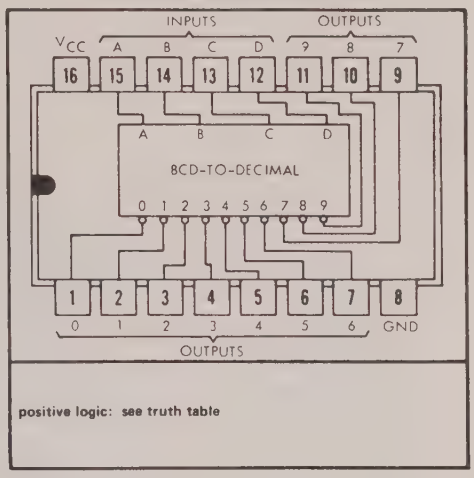
SN5442/SN7442 BCD INPUT				SN5443/SN7443 EXCESS 3 INPUT				SN5444/SN7444 EXCESS 3 GRAY INPUT				ALL TYPES DECIMAL OUTPUT									
D	C	B	A	D	C	B	A	D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	0	0	0	0	0	1	1	0	0	1	0	0	1	1	1	1	1	1	1	1	1
0	0	0	1	0	1	0	0	0	1	1	0	1	0	1	1	1	1	1	1	1	1
0	0	1	0	0	1	0	1	0	1	1	1	1	1	0	1	1	1	1	1	1	1
0	0	1	1	0	1	1	0	0	1	0	1	1	1	1	0	1	1	1	1	1	1
0	1	0	0	0	1	1	1	0	1	0	0	1	1	1	1	0	1	1	1	1	1
0	1	0	1	1	0	0	0	1	1	0	0	1	1	1	1	1	0	1	1	1	1
0	1	1	0	1	0	0	1	1	1	0	1	1	1	1	1	1	1	0	1	1	1
0	1	1	1	1	0	1	0	1	1	1	1	1	1	1	1	1	1	1	0	1	1
1	0	0	0	1	0	1	1	1	1	1	0	1	1	1	1	1	1	1	1	0	1
1	0	0	1	1	1	0	0	1	0	1	0	1	1	1	1	1	1	1	1	1	0
1	0	1	0	1	1	0	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1
1	0	1	1	1	1	1	0	1	0	0	1	1	1	1	1	1	1	1	1	1	1
1	1	0	0	1	1	1	1	1	0	0	0	1	1	1	1	1	1	1	1	1	1
1	1	0	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
1	1	1	0	0	0	0	1	0	0	0	1	1	1	1	1	1	1	1	1	1	1
1	1	1	1	0	0	1	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1

logic

TRUTH TABLE

INPUTS				OUTPUTS									
D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	0	0	0	0	1	1	1	1	1	1	1	1	1
0	0	0	1	1	0	1	1	1	1	1	1	1	1
0	0	1	0	1	1	0	1	1	1	1	1	1	1
0	0	1	1	1	1	1	0	1	1	1	1	1	1
0	1	0	0	1	1	1	1	0	1	1	1	1	1
0	1	0	1	1	1	1	1	1	0	1	1	1	1
0	1	1	0	1	1	1	1	1	1	0	1	1	1
0	1	1	1	1	1	1	1	1	1	1	0	1	1
1	0	0	0	1	1	1	1	1	1	1	1	0	1
1	0	0	1	1	1	1	1	1	1	1	1	1	0
1	0	1	0	1	1	1	1	1	1	1	1	1	1
1	0	1	1	1	1	1	1	1	1	1	1	1	1
1	1	0	0	1	1	1	1	1	1	1	1	1	1
1	1	0	1	1	1	1	1	1	1	1	1	1	1
1	1	1	0	1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1	1	1	1	1

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: see truth table

description

These monolithic BCD-to-decimal decoder/drivers consist of eight inverters and ten four-input NAND gates. The inverters are connected in pairs to make BCD input data available for decoding by the NAND gates. Full decoding of valid BCD input logic ensures that all outputs remain off for all invalid binary input conditions. These decoders feature TTL inputs and high-performance, n-p-n output transistors designed for use as indicator/relay drivers or as open-collector logic-circuit drivers. Each of the high-breakdown output transistors (SN5445, SN7445 = 30 volts and SN54145, SN74145 = 15 volts) will sink up to 80 milliamperes of current. Each input is one normalized Series 54/74 load. Inputs and outputs are entirely compatible for use with TTL or DTL logic circuits, and the outputs are compatible for interfacing with most MOS integrated circuits. Power dissipation is typically 215 milliwatts.

logic

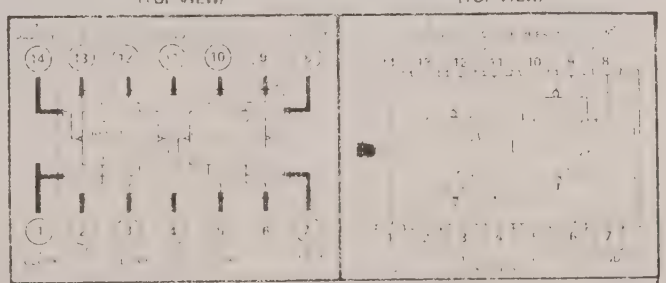
TRUTH TABLE (Each Flip-Flop)

t_n	t_{n+1}	
INPUT	OUTPUT	OUTPUT
D	Q	$\overline{Q}$
0	0	1
1	1	0

NOTES 1. t_n = bit time before clock pulse
2. t_{n+1} = bit time after clock pulse

S FLAT PACKAGE
(TOP VIEW)

J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



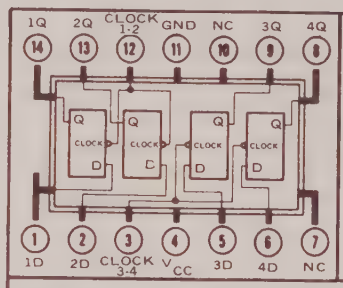
positive logic: Low input to preset sets Q to logical 1
Low input to clear sets Q to logical 0
Preset and clear are independent of clock

logic

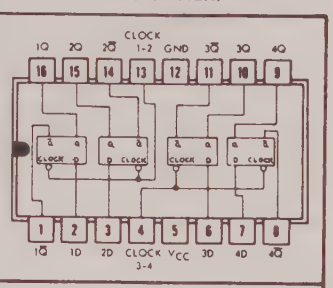
TRUTH TABLE (Each Latch)	
t_n	t_{n+1}
D	Q
1	1
0	0

NOTES. 1. t_n = bit time before clock pulse transition.
2. t_{n+1} = bit time after clock pulse transition.
NC—No Internal Connection

SN5477/SN7477
S FLAT PACKAGE
(TOP VIEW)

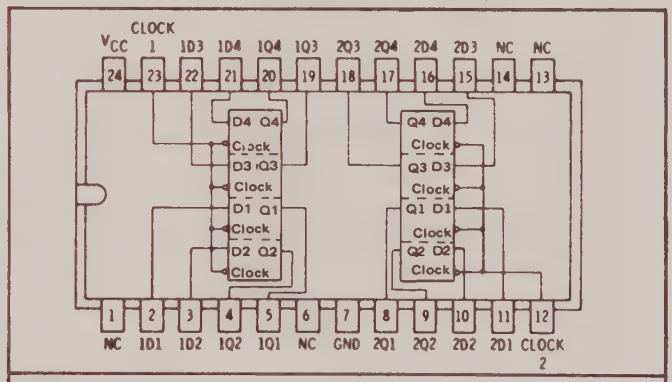


SN5475/SN7475
J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



positive logic: see truth table

SN54100/SN74100
N DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: see truth table

description

These latches are ideally suited for use as temporary storage for binary information between processing units and input/output or indicator units. Information present at a data (D) input is transferred to the Q output when the clock is high, and the Q output will follow the data input as long as the clock remains high. When the clock goes low, the information (that was present at the data input at the time the transition occurred) is retained at the Q output until the clock is permitted to go high.

The SN5475/SN7475 features complementary Q and $\overline{Q}$ outputs from a 4-bit latch, and is available in the 16-pin packages. For higher component density applications the SN5477/SN7477 4-bit latch is available in the 14-pin flat package. The SN54100/SN74100 features two independent quadruple latches in a single 24-pin dual-in-line package.

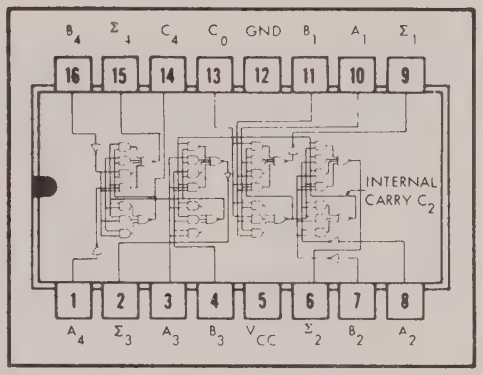
These circuits are completely compatible with all popular TTL or DTL families. Typical power dissipation is 40 milliwatts per latch. The Series 54 circuits are characterized for operation over the full military temperature range of −55°C to 125°C and Series 74 circuits are characterized for operation from 0°C to 70°C.

logic

INPUT				OUTPUT					
				WHEN $C_0 = 0$			WHEN $C_0 = 1$		
				WHEN $C_2 = 0$			WHEN $C_2 = 1$		
A_1 / A_3	B_1 / B_3	A_2 / A_4	B_2 / B_4	Σ_1 / Σ_3	Σ_2 / Σ_4	C_2 / C_4	Σ_1 / Σ_3	Σ_2 / Σ_4	C_2 / C_4
0	0	0	0	0	0	0	1	0	0
1	0	0	0	1	0	0	0	1	0
0	1	0	0	1	0	0	0	1	0
1	1	0	0	0	1	0	1	1	0
0	0	1	0	0	1	0	1	1	0
1	0	1	0	1	1	0	0	0	1
0	1	1	0	1	1	0	0	0	1
1	1	1	0	0	0	1	1	0	1
0	0	0	1	0	1	0	1	1	0
1	0	0	1	1	1	0	0	0	1
0	1	0	1	1	1	0	0	0	1
1	1	0	1	0	0	1	1	0	1
0	0	1	1	0	0	1	1	0	1
1	0	1	1	1	0	1	0	1	1
0	1	1	1	1	0	1	0	1	1
1	1	1	1	0	1	1	1	1	1

NOTE 1: Input conditions at A_1, A_2, B_1, B_2, and C_0 are used to determine outputs Σ_1 and Σ_2, and the value of the internal carry C_2. The values at C_2, A_3, B_3, A_4, and B_4, are then used to determine outputs Σ_3, Σ_4, and C_4.

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



description

This full adder performs the addition of two 4-bit binary numbers. The sum (Σ) outputs are provided for each bit and the resultant carry (C_4) is obtained from the fourth bit. Designed for medium-to-high-speed, multiple-bit, parallel-add/serial-carry applications, the circuit utilizes high-speed, high-fan-out transistor-transistor logic (TTL) but is compatible with both DTL and TTL families. The implementation of a single-inversion, high-speed, Darlington-connected serial-carry circuit within each bit minimizes the necessity for extensive "look-ahead" and carry-cascading circuits. The power dissipation level has been maintained considerably below that attainable with equivalent standard integrated circuits connected to perform four-bit full-adder functions.

MSI TTL HIGH-SPEED DECADE COUNTERS

for applications in

- Digital Computer Systems
- Data-Handling Systems
- Control Systems

logic

TRUTH TABLES

BCD COUNT SEQUENCE
(See Note 1)

COUNT	OUTPUT D	C	B	A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1

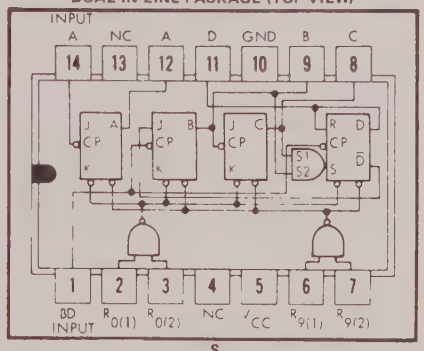
RESET/COUNT (See Note 2)

RESET INPUTS $R_{0(1)}$	$R_{0(2)}$	$R_{9(1)}$	$R_{9(2)}$	OUTPUT D C B A
1	1	0	X	0 0 0 0
1	1	X	0	0 0 0 0
X	X	1	1	1 0 0 1
X	0	X	0	COUNT
0	X	0	X	COUNT
0	X	X	0	COUNT
X	0	0	X	COUNT

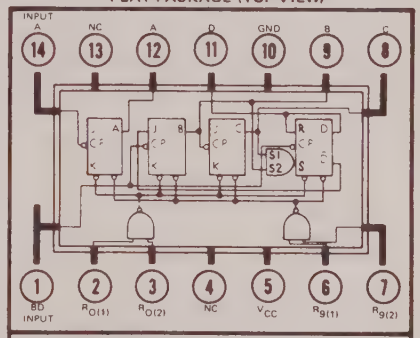
NC – No Internal Connection

NOTES. 1. Output A connected to input BD for BCD count.
2. X indicates that either a logical 1 or a logical 0 may be present.

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



S
FLAT PACKAGE (TOP VIEW)



positive logic: see truth table

description and typical count configurations

These high-speed, monolithic decade counters consist of four dual-rank, master-slave flip-flops internally interconnected to provide a divide-by-two counter and a divide-by-five counter. Gated direct reset lines are provided to inhibit count inputs and return all outputs to logical zero or to a binary coded decimal (BCD) count of 9. As the output from flip-flop A is not internally connected to the succeeding stages, the count may be separated in three independent count modes:

1. When used as a binary coded decimal decade counter, the BD input must be externally connected to the A output. The A input receives the incoming count, and a count sequence is obtained in accordance with the BCD count sequence truth table shown above. In addition to a conventional zero reset, inputs are provided to reset a BCD count for nine's complement decimal applications.

2. If a symmetrical divide-by-ten count is desired for frequency synthesizers or other applications requiring division of a binary count by a power of ten, the D output must be externally connected to the A input. The input count is then applied at the BD input and a divide-by-ten square wave is obtained at output A.

3. For operation as a divide-by-two counter and a divide-by-five counter, no external interconnections are required. Flip-flop A is used as a binary element for the divide-by-two function. The BD input is used to obtain binary divide-by-five operation at the B, C, and D outputs. In this mode, the two counters operate independently; however, all four flip-flops are reset simultaneously.

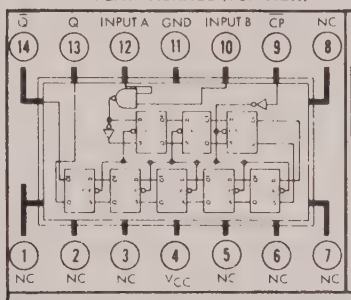
These circuits are completely compatible with Series 54/74 TTL and DTL logic families. Average power dissipation is 160 mW.

logic

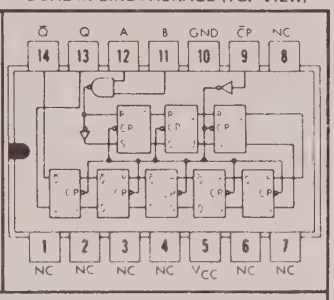
t_n		t_{n+8}
A	B	Q
0	0	0
0	1	0
1	0	0
1	1	1

NOTES:
1. t_n = bit time before clock.
2. t_{n+8} = bit time after 8 clock pulses.

S
FLAT PACKAGE (TOP VIEW)



J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: See Truth Table

NC—No Internal Connection

description

These monolithic serial-in, serial-out, 8-bit shift registers utilizing transistor-transistor logic (TTL) circuits, are composed of eight R-S master-slave flip-flops, input gating, and a clock driver. The register is capable of storing and transferring data at clock rates up to 18 MHz while maintaining a typical noise-immunity level of 1 volt. Power dissipation is typically 175 milliwatts, and a full fan-out of 10 is available from the outputs.

Single-rail data and input control are gated through inputs A and B and an internal inverter to form the complementary inputs to the first bit of the shift register. Drive for the internal common clock line is provided by an inverting clock driver. Each of the inputs (A, B, and $\overline{CP}$) appear as only one TTL input load.

The clock pulse inverter/driver causes these circuits to shift information to the output on the positive edge of an input clock pulse, thus enabling the shift-register to be fully compatible with other edge-triggered synchronous functions.

description

This shift register consists of five R-S master-slave flip-flops connected to perform parallel-to-serial or serial-to-parallel conversion of binary data. Since both inputs and outputs to all flip-flops are accessible, parallel-in/parallel-out or serial-in/serial-out operation may be performed.

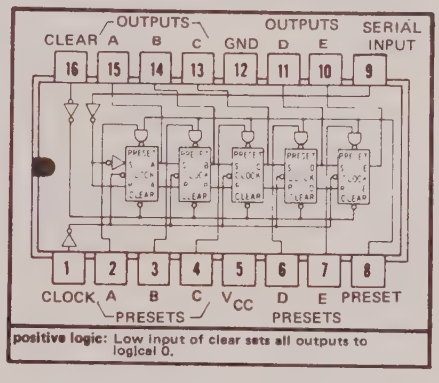
All flip-flops are simultaneously set to the logical 0 state by applying a logical 0 voltage to the clear input. This condition may be applied independent of the state of the clock input.

The flip-flops may be independently set to the logical 1 state by applying a logical 1 to both the preset input of the specific flip-flop and the common preset input. The common preset input is provided to allow flexibility of either setting each flip-flop independently or setting two or more flip-flops simultaneously. Preset is also independent of the state of the clock input or clear input.

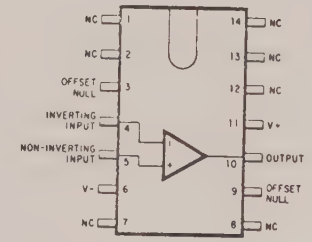
Transfer of information to the output pins occurs when the clock input goes from a logical 0 to a logical 1. Since the flip-flops are R-S master-slave circuits, the proper information must appear at the R-S inputs of each flip-flop prior to the rising edge of the clock input voltage waveform. The serial input provides this information to the first flip-flop, while the outputs of the subsequent flip-flops provide information for the remaining R-S inputs. The clear input must be at a logical 1 and the preset input must be at a logical 0 when clocking occurs.

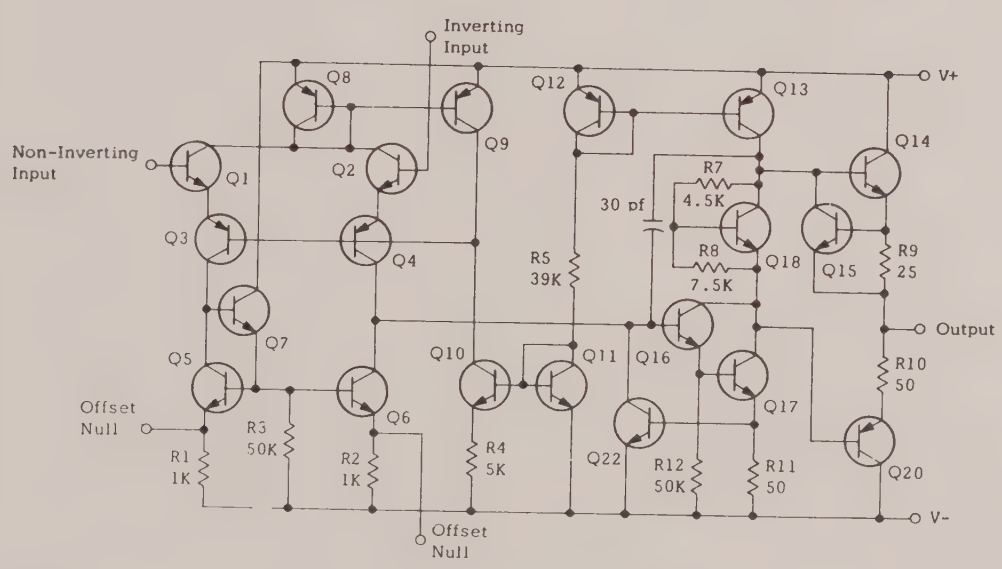
This shift register is completely compatible with Series 54/74 TTL and DTL logic families. Typically, average power dissipation is 240 milliwatts, and propagation delay time is 25 nanoseconds.

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: Low input of clear sets all outputs to logical 0.


NC
NC
OFFSET NULL
INVERTING INPUT
NON-INVERTING INPUT
V-
NC
1
2
3
4
5
6
7
14
13
12
11
10
9
8
NC
NC
NC
V+
OUTPUT
OFFSET NULL
NC


Inverting Input
Non-Inverting Input
Offset Null
Offset Null
Output
V+
V-
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
Q9
Q10
Q11
Q12
Q13
Q14
Q15
Q16
Q17
Q18
Q20
Q22
R1 1K
R2 1K
R3 50K
R4 5K
R5 39K
R7 4.5K
R8 7.5K
R9 25
R10 50
R11 50
R12 50K
30 pf

SECTION 11

RECOMMENDED SPARE PARTS LIST

Dana Part No.	Manufacturer Part No.	Qty.
230028	IC SN7400N	2
230030	IC SN7402N	1
230031	IC SN7410N	1
230032	IC SN7420N	1
230033	IC SN7430N	1
350005	IC SN7474N	2
230036	IC SN7483N	1
230037	IC SN7490N	1
350007	IC SN7491AN	1
230043	IC MC1010P	1
230040	IC MC1013P	1
230034	IC SN7441N	2
350006	IC SN7475N	1
350015	IC SN7442N	1
350018	IC SN7496N	1

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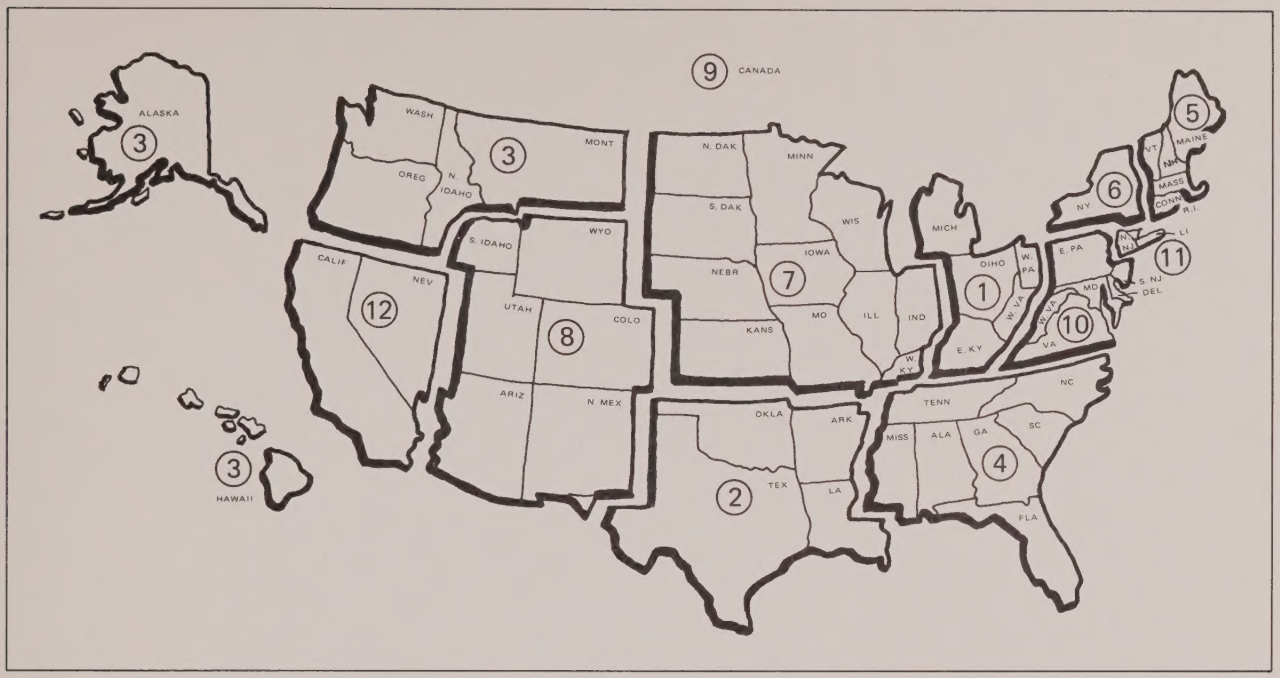

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